GENERAL DESCRIPTION

The XP8003/XP8003F is a high-efficiency monolithic synchronous buck regulator using a constant frequency, Constant On-Time (COT) mode architecture.

Quiescent current of XP8003 is 35μA, and when it is turn off , shutdown current is below 1μA.With an input voltage range of 2.5V to 6V, it is highly suitable for applications powered by a single lithium-ion battery. A 100% duty cycle enables low dropout operation, thereby extending the battery life of portable systems.

DCM/CCM mode operation provides very low output ripple voltage for noise sensitive applications. Switching frequency is internally set at 1.0MHz for XP8003, FCCM mode operation for XP8003F, allowing the use of small surface mount inductors and capacitors. Low output voltages are easily supported with the 0.6V feedback reference voltage.

The XP8003/XP8003F requires a minimal number of readily available, external components and is available in a small package.

FEATURES

- Wide 2.5V to 6V Operating Input Range
- 3A Continuous Output Current
- 1.0MHz Switching Frequency
- 35uA Low Quiescent Current
- Short Protection with Hiccup-Mode
- Built-in overcurrent Limit
- DCM for High Efficiency in Light Load Condition (XP8003)
- FCCM for Low noise (XP8003F)
- Integrated internal Soft-Start
- 90/50mΩ Low $R_{DS(ON)}$ Internal MOSFETs
- Output Adjustable from 0.6V
- Input OVP 6.3V
- 100% Duty cycle
- Built-in 35Ω Discharge Resistor
- Thermal Shutdown
- COT Mode
- SOT23-5 Package

APPLICATIONS

- STB, SSD, PC, Audio
- XDSL AP and Router
- IP Cameras
- TV and Monitor
- Smart Home

TYPICAL APPLICATION CIRCUIT

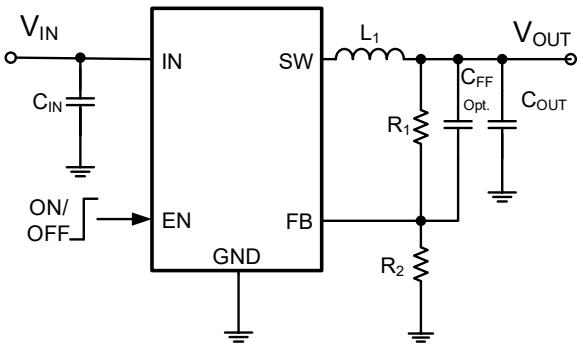
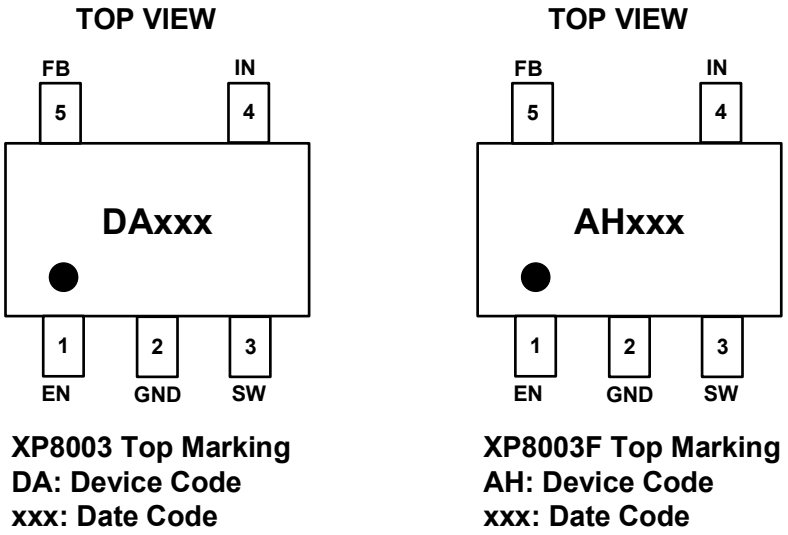


Figure 1. Basic Application Circuit

MARKING/PINOUT INFORMATION



XP8003 Top Marking
DA: Device Code
xxx: Date Code

XP8003F Top Marking
AH: Device Code
xxx: Date Code

Figure 2. Marking/Pinout Information

PIN DESCRIPTION

SOT23-5	Name	Function
1	EN	Chip Enable Pin. Drive EN above 1.2V to turn on the part. Drive EN below 0.4V to turn it off. Do not leave EN floating.
2	GND	Ground Pin.
3	SW	Power Switch Output. It is the switch node connection to Inductor. This pin connects to the drains of the internal P-ch and N-ch MOSFET switches.
4	IN	Power Supply Input. Must be closely decoupled to GND with a 10µF or greater ceramic capacitor.
5	FB	Output Voltage Feedback Pin. An internal resistive divider divides the output voltage down for comparison to the internal reference voltage.

ORDER INFORMATION (1)

Part No.	Description	Temperature	Package	T/R Qty
XP8003	2.5-6V, 3A, 1.0MHz, VFB 0.6V, **DCM**	-40°C-125°C	SOT23-5	3000PCS
XP8003F	2.5-6V, 3A, 1.0MHz, VFB 0.6V, **FCCM**	-40°C-125°C	SOT23-5	3000PCS

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (1) (2)

Item	Min	Max	Unit
IN voltage	-0.3	6.5	V
EN voltage	-0.3	6.5	V
SW voltage	-3.0 (<10ns)	VIN+1.5V (<10ns)	V
FB voltage	–0.3	6.5	V
Power dissipation	Internally Limited		
Operating junction temperature, TJ	-40	150	°C
Storage temperature, Tstg	–65	150	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

RECOMMENDED OPERATING CONDITIONS (1)

Item	Min	Max	Unit
Operating junction temperature (1)	–40	125	°C
Operating temperature range	-40	85	°C
Input voltage VIN	2.5	6	V
Output current	0	3	A

Note (1): All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

THERMAL INFORMATION (1)

Item	Description	SOT23-5	Unit
RθJA	Junction-to-ambient thermal resistance	200	°C/W
RθJC(top)	Junction-to-case (top) thermal resistance	130	°C/W

ESD RATINGS

Item	Description	Value	Unit
HBM	Human-body model, per ANSI/ESDA/JEDEC JS-001	±2000	V
CDM	Charged-device model, per ANSI/ESDA/JEDEC JS-002	±1000	V

ELECTRICAL CHARACTERISTICS (1)

(XP8003) VIN=5V, TA=25°C, unless otherwise specified.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Voltage Range		2.5		6.0	V
VIN Under-Voltage Lockout Rising Threshold			2.4		V
VIN Under-Voltage Lockout Hysteresis			300		mV
Quiescent current into VIN(XP8003)	V_{IN}=5.0V, No Switching, V_{FB}=0.65V		35		μA
Quiescent current into VIN(XP8003F)	V_{IN}=5.0V, No Switching, V_{FB}=0.65V		66		uA
Shutdown current into VIN	V_{EN}=0V, V_{IN}=5V			1	μA
Regulated Feedback Voltage	V_{IN}=5V, TA=25°C	0.588	0.600	0.612	V
Oscillation Frequency	V_{IN}=5V, V_{OUT}=1.8V, Iload=1A		1.0		MHz
On Resistance of PMOS	I_{SW}= 100mA		90		mΩ
ON Resistance of NMOS	I_{SW}=-100mA		50		mΩ
High-Side Switch Current Limit			5.0		A
Low-Side Switch Current Limit			4.0		A
EN Rising Threshold		1.2			V
EN Falling Threshold				0.4	V
SW Leakage Current	V_{EN}=0V, V_{IN}=V_{SW}=5V			1	μA
Soft Start Time	V_{OUT}:10%~90%		0.6		ms
Hiccup on Time			1		ms
Hiccup Time Before Restart			15		ms
Output Discharger Resistance	V_{IN}=5V, V_{EN}=0V		35		Ω
Thermal Shutdown Threshold			160		℃
Thermal Shutdown Hysteresis			20		℃

Note (1): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

FUNCTIONAL BLOCK DIAGRAM

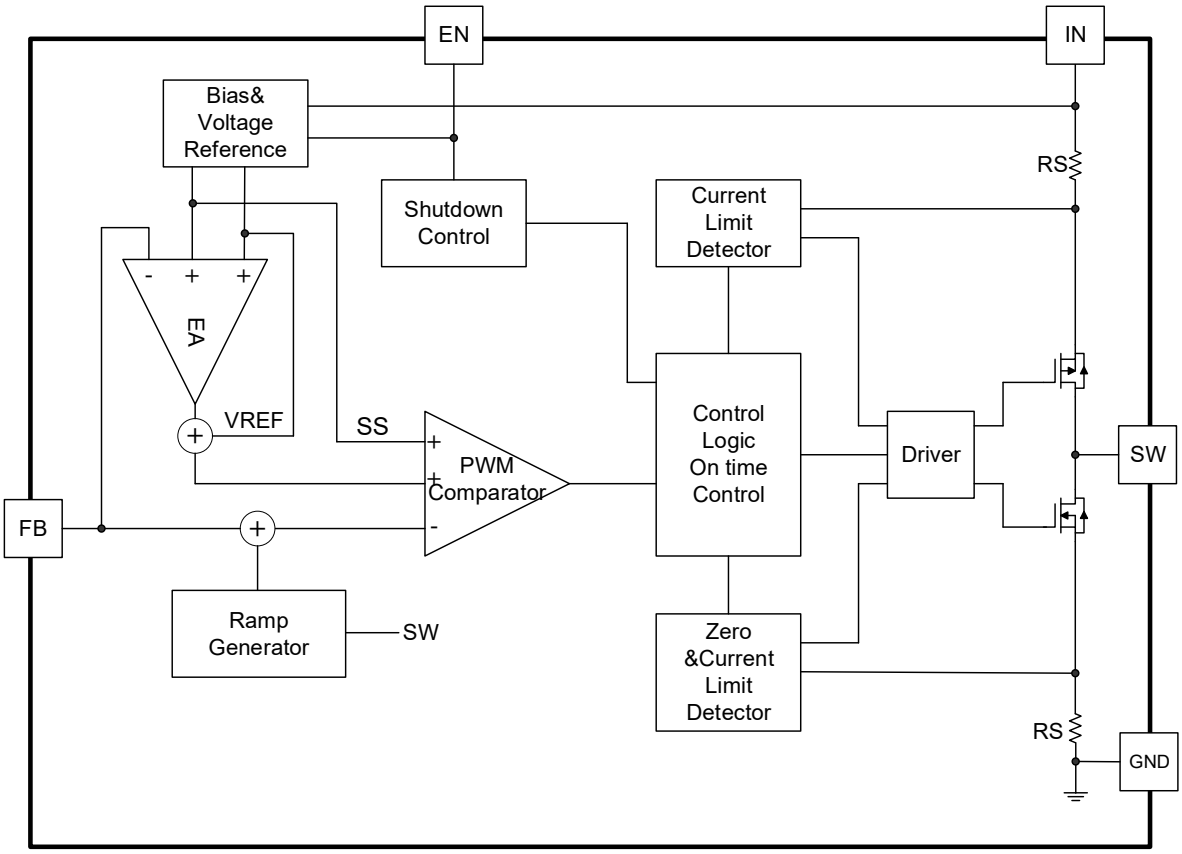


Figure 3. Block Diagram

FUNCTIONS DESCRIPTION

OVERVIEW

The XP8003/XP8003F is a COT mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains an internal, low resistance, high voltage power MOSFET, and operates at a high 1.0MHz operating frequency to ensure a compact, high efficiency design with excellent performance.

STARTUP AND SHUTDOWN

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and bias current, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Four events can shut down the chip: EN low, VIN_UV, VIN_OV and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The comp voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

UNDER-VOLTAGE LOCKOUT (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

INPUT OVER-VOLTAGE PROTECTION

XP8003/XP8003F monitors the input voltage to achieve overvoltage protection at the input end. When the input voltage exceeds 6.3V, the chip stops operating, and when the input voltage drops below 6.29V, the chip resumes operation.

THERMAL SHUTDOWN

The device features auto-recovery mode over temperature protection to guarantee IC safe operation when the internal power MOSFET regulator power loss is great. Once the power MOSFET thermal sensor detects that power MOSFET junction temperature exceeds 160°C, the device will be turned off. When the power MOSFET junction temperature cools down by approximately 20°C, the device will be recovered again.

INTERNAL SOFT-START

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 0.6V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control. The SS time is internally to 0.6ms (Typ.).

OVER-CURRENT-PROTECTION AND SHORT CIRCUITS PROTECTION

The XP8003/XP8003F has a cycle-by-cycle over-current limiting control (OCL). The current-limit circuit employs a valley current-sensing algorithm. The part uses the RDS(ON) of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, PWM is not allowed to initiate a new cycle, even if FB is lower than REF.

Since the comparison is done during the LS-FET on state, the OC trip level sets the valley level of the inductor current. The maximum load current at the over-current threshold (IOC) can be calculated using the following equation:

$$I_{OC} = I_limit + \frac{\Delta I_{inductor}}{2}$$

The OCL itself limits the inductor current and does not latch off. In an over-current condition, the current to the load exceeds the current to the output capacitor, causing the output voltage to fall off. Eventually, the VFB drops below the under-voltage protection (UVP) threshold, XP8003/XP8003F will enter hiccup protection.

ZERO-CROSSING DETECTION (XP8003)

The XP8003 device uses a zero-crossing (ZC) circuit to perform the zero-inductor current detection during skip-mode operation. The ZC threshold is set to a small positive value before the low-side MOSFET is turned off to compensate for delay in the ZC detection circuit, entering discontinuous conduction mode (DCM) operation.

OUTPUT DISCHARGE

During EN shutdown, IC will enter discharge mode automatically, there is an internal discharge MOSFET provide a resistive discharge path for the output capacitor, the discharge resistance is 35Ω, and the typical discharge time is 20ms.

APPLICATIONS INFORMATION

SETTING THE OUTPUT VOLTAGE

XP8003/XP8003F require an input capacitor, an output capacitor and an inductor. These components are critical to the performance of the device. XP8003/XP8003F are internally compensated and do not require external components to achieve stable operation. The output voltage can be programmed by resistor divider.

$$V_{OUT} = V_{FB} \times \frac{R1 + R2}{R2}$$

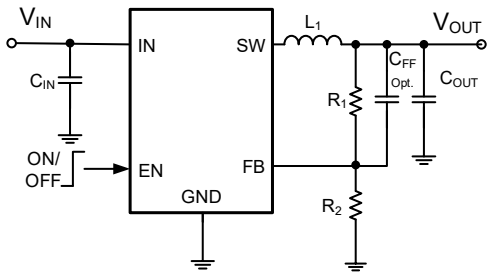


Figure 4. Typical Application

EXAMPLE OF COMPONENT SELECTION

VOUT(V)	R1(kΩ)	R2(kΩ)	L1(μH)	CIN(μF)	COUT(μF)	CFF (pF) Opt.
1.0	6.67	10	1.0	10	22+10	10-100
1.2	10.00	10	1.0	10	22+10	10-100
1.5	15.00	10	1.0	10	22+10	10-100
1.8	20.00	10	1.0	10	22+10	10-100
3.3	45.30	10	1.0	10	22+10	10-100

SELECTING THE INDUCTOR

The recommended inductor values are shown in the Application Diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the peak load current plus the ripple current: Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where ΔIL is the inductor ripple current. Choose inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

SELECTING THE INPUT CAPACITOR

CIN The ripple current through input capacitor is calculated as:

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

To minimize the potential noise problem, a typical X5R or better grade ceramic capacitor with 6.3V rating should be placed really close to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins. In this case, a 10μF low ESR ceramic capacitor is recommended

SELECTING THE OUTPUT CAPACITOR

Special attention should be paid when selecting these components. The DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table.

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R or better grade ceramic capacitor with 6.3V rating and more than 22μF or 22μF+10μF capacitance.

PCB LAYOUT EXAMPLE & GUIDELINES

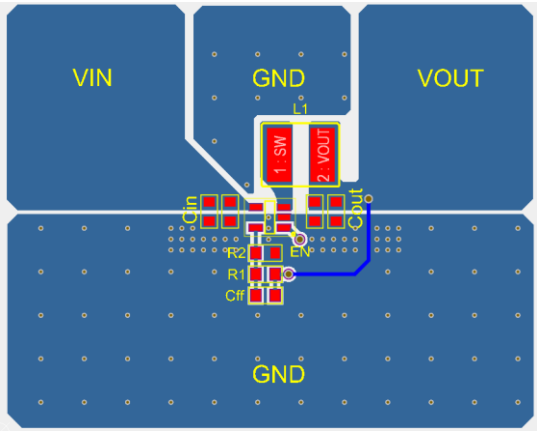


Figure 5. SOT23-5 Layout

The PCB layout is an important step to maintain the high performance of the XP8003/XP8003F device.

1. The input/output capacitors and the inductor should be placed as close as possible to the IC. This keeps the power traces short. Routing these power traces direct and wide results in low trace resistance and low parasitic inductance.
2. The low side of the input and output capacitors must be connected properly to the power GND to avoid a GND potential shift.
3. The sense traces connected to FB are signal traces. Special care should be taken to avoid noise being induced. Keep these traces away from SW nodes.
4. GND layers might be used for shielding.

PACKAGE DESCRIPTION

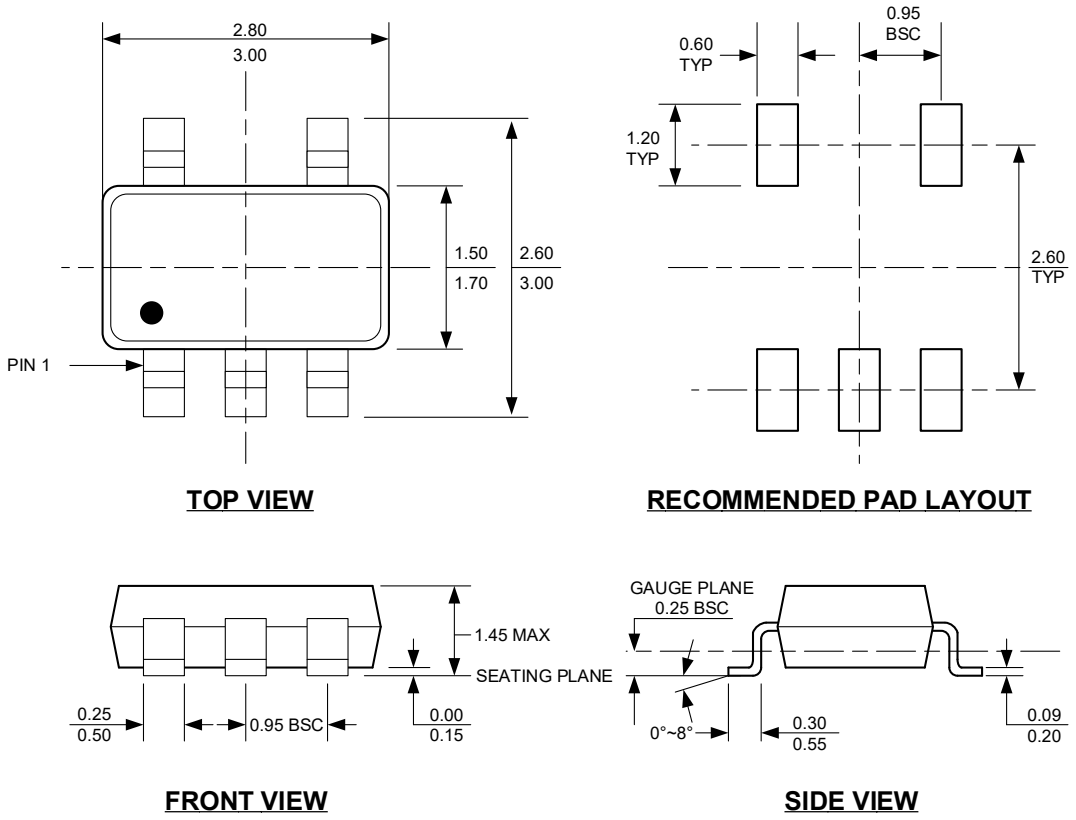
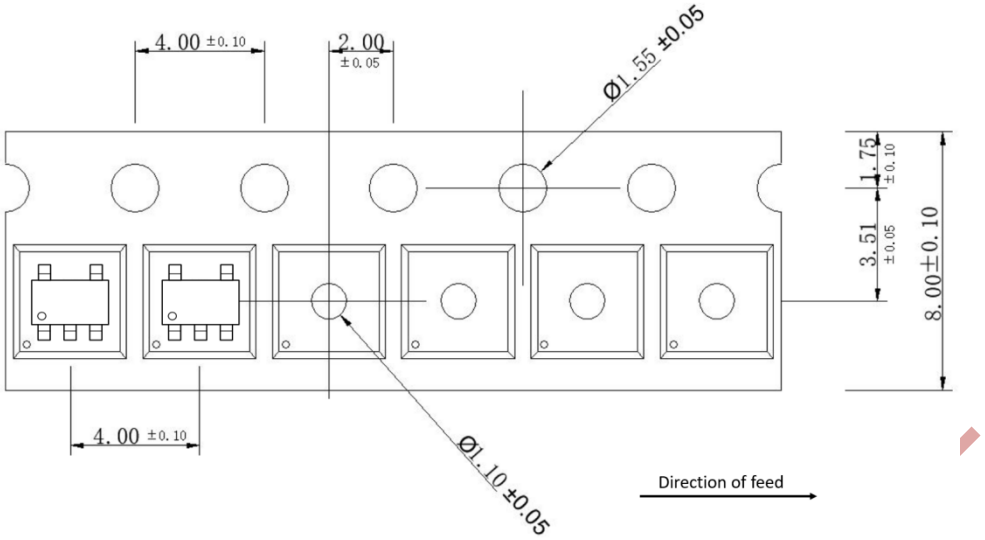


Figure 6. SOT23-5 Package Description

NOTE:

1. CONTROL DIMENSIONS IS IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION



REEL DIMENSIONS

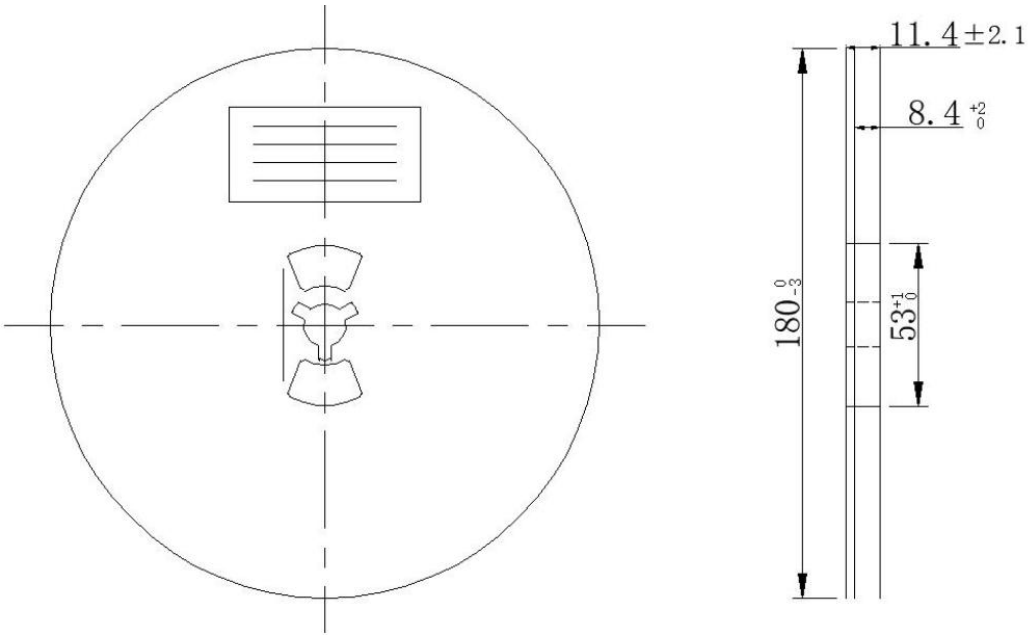


Figure 7. SOT23-5 Tape and Reel Information

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. QUANTITY OF UNITS PER REEL IS 3000.
3. MSL LEVEL IS LEVEL 3.