GENERAL DESCRIPTION

The XR8303B/XR8303BF is a high-efficiency monolithic synchronous step-down DC/DC converter that operates from a 4V to 32V input voltage and can deliver up to 3A of continuous output current. The supply current of the XR8303B is 200μA when there is no load, and drops to <3μA when it is turned off.

DCM/CCM mode operation provides very low output ripple voltage for noise sensitive applications. Switching frequency is internally set at 600kHz for XR8303B, FCCM mode operation for XR8303BF, allowing the use of small surface mount inductors and capacitors. Low output voltages are easily supported with the 0.925V feedback reference voltage.

The XR8303B/XR8303BF requires a minimal number of readily available, external components and is available in a small package.

FEATURES

- Wide 4V to 32V Operating Input Range
- 3A Continuous Output Current
- 600kHz Switching Frequency
- Short Protection with Hiccup-Mode
- Built-in overcurrent Limit
- DCM for High Efficiency in Light Load Condition (XR8303B)
- FCCM for Low noise (XR8303BF)
- Integrated internal Soft-Start
- 140/90mΩ Low $R_{DS(ON)}$ internal MOSFETs
- Output Adjustable from 0.925V
- Low EMI Signature
- 100% Duty cycle Max
- Thermal Shutdown
- COT Mode
- ESOP-8 Package

APPLICATIONS

- Automotive Entertainment
- Wireless and DSL Modems
- Computer Entertainment
- IoT Applications
- Digital Still and Video Cameras

TYPICAL APPLICATION CIRCUIT

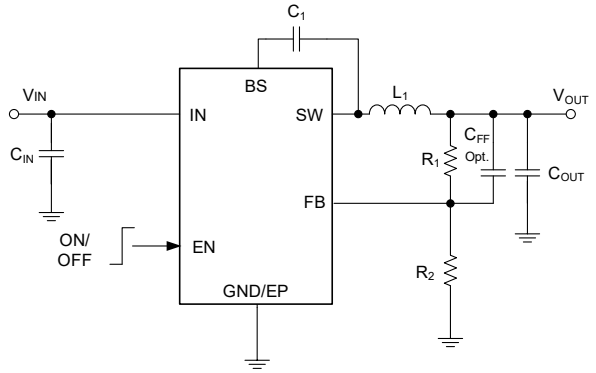


Figure 1. Typical Application Circuit

MARKING/PINOUT INFORMATION



8303B: Device Code
xxxx : Date Code



8303BF: Device Code
xxxx : Date Code

Figure 2. Marking Information

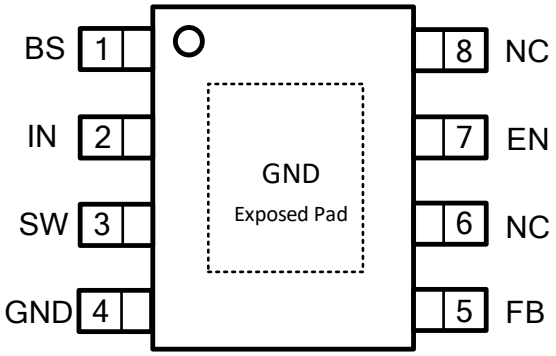


Figure 3. Pinout Information

PIN DESCRIPTION

ESOP-8	Name	Function
1	BS	Bootstrap pin. A capacitor connected between SW and BS pin is required to form a floating supply across the high-side switch driver.
2	IN	Power supply pin.
3	SW	Switching pin.
4	GND	Ground pin.
5	FB	Output Voltage feedback input pin. Connect FB to the center point of the external resistor divider.
6	NC	Not Connected.
7	EN	Enable pin. Drive this pin to a logic-high to enable the IC. Drive to a logic-low to disable the IC and enter micro-power shutdown mode.
8	NC	Not Connected.
Exposed Pad	GND	Ground pin.

ORDER INFORMATION (1)

Part No.	Description	Temperature	Package	T/R Qty
XR8303B	4-32V, 3A, 600kHz, VFB 0.925V, **DCM**	-40°C-125°C	ESOP-8	4000pcs
XR8303BF	4-32V, 3A, 600kHz, VFB 0.925V, **FCCM**	-40°C-125°C	ESOP-8	4000pcs

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (1) (2)

Item	Min	Max	Unit
IN voltage	-0.3	36	V
EN voltage	-0.3	36	V
SW voltage	-0.3	36	V
BS -SW voltage	-0.3	6	V
FB voltage	–0.3	6	V
SS voltage	–0.3	6	V
Operating junction temperature, TJ	-40	125	°C
Storage temperature, Tstg	–65	150	°C
Lead Temperature (Soldering, 10sec.)		260	°C

Note (1): Exceeding these ratings may damage the device.

Note (2): The device is not guaranteed to function outside of its operating conditions.

RECOMMENDED OPERATING CONDITIONS (1)

Item	Min	Max	Unit
Operating junction temperature (1)	–40	125	°C
Operating temperature range	-40	85	°C
Input voltage VIN	4	32	V
Output current	0	3.0	A

Note (1): All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

THERMAL INFORMATION (1)

Item	Description	ESOP-8	Unit
RθJA	Junction-to-ambient thermal resistance	49	°C/W
RθJC (top)	Junction-to-case (top) thermal resistance	35	°C/W

ESD RATINGS

Item	Description	VALUE	Unit
HBM	Human-body model, per ANSI/ESDA/JEDEC JS-001	±2000	V
CDM	Charged-device model, per ANSI/ESDA/JEDEC JS-002	±1000	V

ELECTRICAL CHARACTERISTICS (1)

VIN=12V, Vout=5V, TA=25°C, unless otherwise specified.

Parameter	Conditions	Min.	Typ.	Max.	Unit
Input Voltage Range		4		32	V
VIN Under-Voltage Lockout Rising Threshold			3.5		V
VIN Under-Voltage Lockout Hysteresis			500		mV
Quiescent current (XR8303B)	V_{IN}=12V, No Switching, V_{FB}=1V		200		μA
Quiescent current (XR8303BF)	V_{IN}=12V, No Switching, V_{FB}=1V		200		μA
Shutdown current	V_{EN} = 0V, V_{IN} = 12V		1		μA
Regulated Feedback Voltage	T_A=25°C	0.915	0.925	0.935	V
High-Side Switch On-Resistance			140		mΩ
Low-Side Switch On-Resistance			90		mΩ
High-Side Switch Leakage Current	V_{EN}=0V, V_{SW}=0V			1.0	μA
Low-Side Valley Current Limit			5		A
Oscillation Frequency			600		kHz
Maximum Duty Cycle			100		%
Minimum On-Time			60		ns
Soft Start	V_{OUT}:10%~90%		1.9		ms
Hiccup on Time			3.5		ms
Hiccup Time Before Restart			46.5		ms
EN Rising Threshold			1.1		V
EN Hysteresis			0.16		V
Thermal Shutdown Threshold			160		°C
Thermal Shutdown Hysteresis			20		°C

Note (1): Thermal shutdown specifications are guaranteed by correlation to the design and characteristics analysis.

FUNCTIONAL BLOCK DIAGRAM

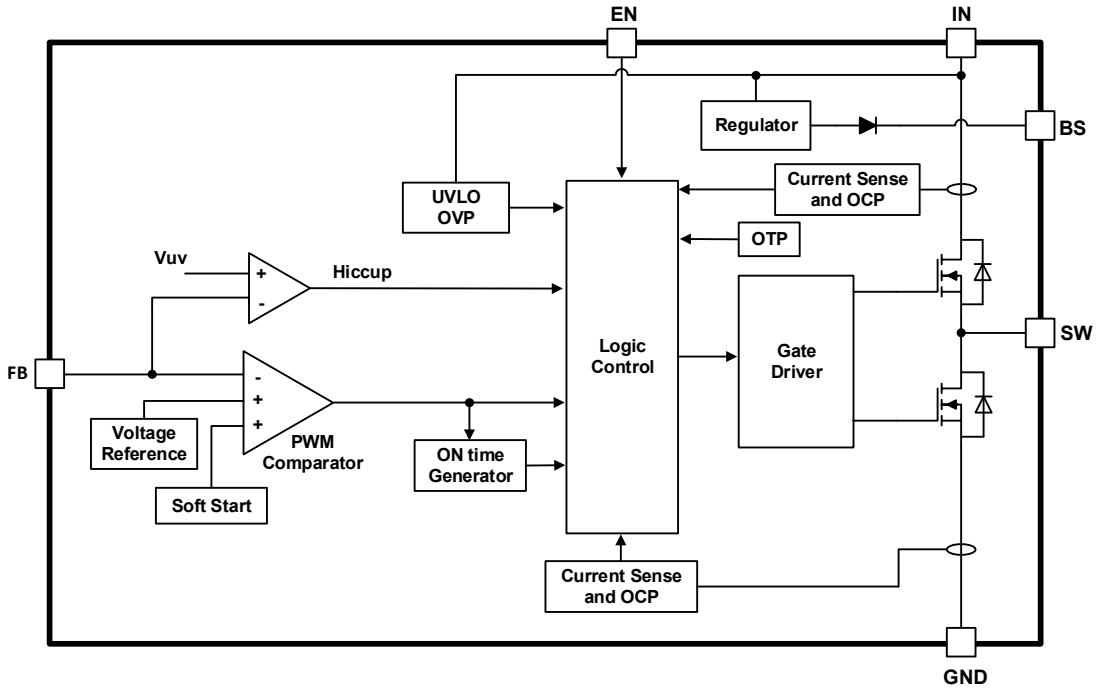


Figure 4. Block Diagram

FUNCTIONS DESCRIPTION

OVERVIEW

The XR8303B/XR8303BF is a COT mode step down DC/DC converter that provides excellent transient response with no extra external compensation components. This device contains internal, low resistance, high voltage power MOSFETs, and operates at a 600kHz operating frequency to ensure a compact, high efficiency design with excellent performance.

STARTUP AND SHUTDOWN

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and bias current, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries. Three events can shut down the chip: EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The comp voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

UNDER-VOLTAGE LOCKOUT (UVLO)

Under-voltage lockout (UVLO) protects the chip from operating at an insufficient supply voltage. UVLO protection monitors the internal regulator voltage. When the voltage is lower than UVLO threshold voltage, the device is shut off. When the voltage is higher than UVLO threshold voltage, the device is enabled again.

INTERNAL SOFT-START

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to VREF. When it is lower than the internal FB reference (VREF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than VREF, VREF regains control. The SS time is internally fixed to 1.9ms typically.

THERMAL SHUTDOWN

The device features auto-recovery mode over temperature protection to guarantee IC safe operation when the internal power MOSFET regulator power loss is great. Once the power MOSFET thermal sensor detects that power MOSFET junction temperature exceeds 160°C, the device will be turned off. When the power MOSFET junction temperature cools down by approximately 20°C, the device will be recovered again.

OVER-CURRENT-PROTECTION AND SHORT CIRCUITS PROTECTION

The XR8303B/XR8303BF has a cycle-by-cycle over-current limiting control (OCL). The current-limit circuit employs a valley current-sensing algorithm. The part uses the RDS(ON) of the LS-FET as a current-sensing element. If the magnitude of the current-sense signal is above the current-limit threshold, PWM is not allowed to initiate a new cycle, even if FB is lower than REF.

Since the comparison is done during the LS-FET on state, the OC trip level sets the valley level of the inductor current. The maximum load current at the over-current threshold (IOC) can be calculated using the following equation:

$$I_{OC} = I_limit + \frac{\Delta I_{inductor}}{2}$$

The OCL itself limits the inductor current and does not latch off. In an over-current condition, the current to the load exceeds the current to the output capacitor, causing the output voltage to fall off. Eventually, the VFB drops below the under-voltage protection (UVP) threshold, XR8303B/XR8303BF will enter hiccup protection.

ZERO-CROSSING DETECTION(XR8303B)

The XR8303B device uses a zero-crossing (ZC) circuit to perform the zero-inductor current detection during skip-mode operation. The ZC threshold is set to a small positive value before the low-side MOSFET is turned off to compensate for delay in the ZC detection circuit, entering discontinuous conduction mode (DCM) operation.

APPLICATIONS INFORMATION

SETTING THE OUTPUT VOLTAGE

XR8303B/XR8303BF requires an input capacitor, an output capacitor and an inductor. These components are critical to the performance of the device. XR8303B/XR8303BF is internally compensated and does not require external components to achieve stable operation.
The output voltage can be programmed by resistor divider.

$$V_{OUT} = V_{FB} \times \frac{R1 + R2}{R2}$$

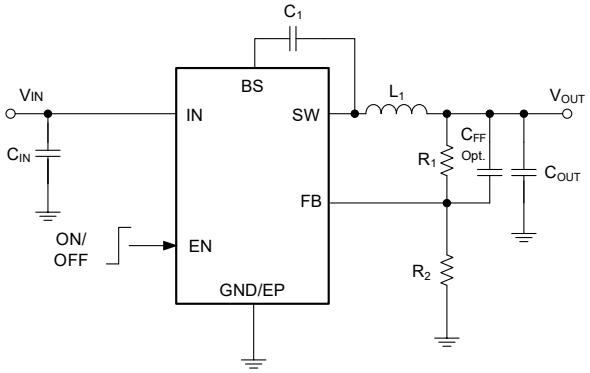


Figure 5. Typical Application

EXAMPLE OF COMPONENT SELECTION

VOUT(V)	R1(kΩ)	R2(kΩ)	L1(μH)	CIN(μF)	COUT(μF)	CFF (pF) Opt.
1.0	0.82	10	1.5	Ec_100+10	22	10-100
1.5	6.2	10	2.2	Ec_100+10	22	10-100
2.5	17	10	3.3	Ec_100+10	22	10-100
3.3	25.5	10	3.3	Ec_100+10	22	10-100
5.0	44.2	10	4.7	Ec_100+10	22	10-100

SELECTING THE INDUCTOR

The recommended inductor values are shown in the Application Diagram. It is important to guarantee the inductor core does not saturate during any foreseeable operational situation. The inductor should be rated to handle the peak load current plus the ripple current: Care should be taken when reviewing the different saturation current ratings that are specified by different manufacturers. Saturation current ratings are typically specified at 25°C, so ratings at maximum ambient temperature of the application should be requested from the manufacturer.

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times F_{OSC}}$$

Where ΔIL is the inductor ripple current. Choose inductor ripple current to be approximately 30% of the maximum load current. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improved efficiency.

SELECTING THE INPUT CAPACITOR

CIN The ripple current through input capacitor is calculated as:

$$I_{CIN_RMS} = I_{OUT} \times \sqrt{D(1-D)}$$

To minimize the potential noise problem, a typical X5R or better grade ceramic capacitor should be placed as close as possible to the IN and GND pins. Care should be taken to minimize the loop area formed by CIN, and IN/GND pins.

SELECTING THE OUTPUT CAPACITOR

Special attention should be paid when selecting these components. The DC bias of these capacitors can result in a capacitance value that falls below the minimum value given in the recommended capacitor specifications table.

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor. For the best performance, it is recommended to use an X5R and more than 22μF capacitance.

PCB LAYOUT GUIDELINES

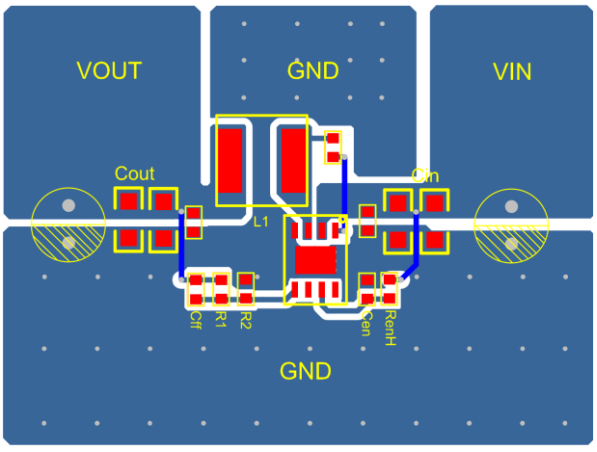


Figure 6. XR8303B/XR8303BF Layout

PCB layout is very important to achieve stable operation. It is highly recommended to duplicate EVB layout for optimum performance. If change is necessary, please follow these guidelines:

1) Keep the path of switching current short and minimize the loop area formed by Input capacitor, IN pin and GND.

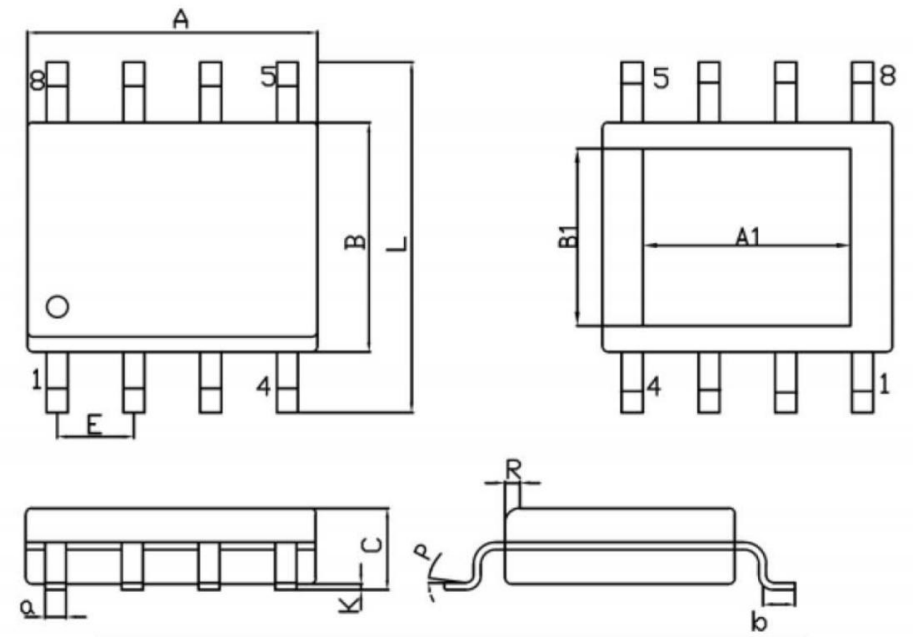
2) Bypass ceramic capacitors are suggested to be put close to the IN Pin.

3) Ensure all feedback connections are short and direct. Place the feedback resistors as close to the chip as possible.

4) Keep BS and SW away from sensitive analog areas such as FB.

5) Connect IN, SW, and especially GND respectively to a large copper area to cool the chip to improve thermal performance and long-term reliability.

PACKAGE DESCRIPTION



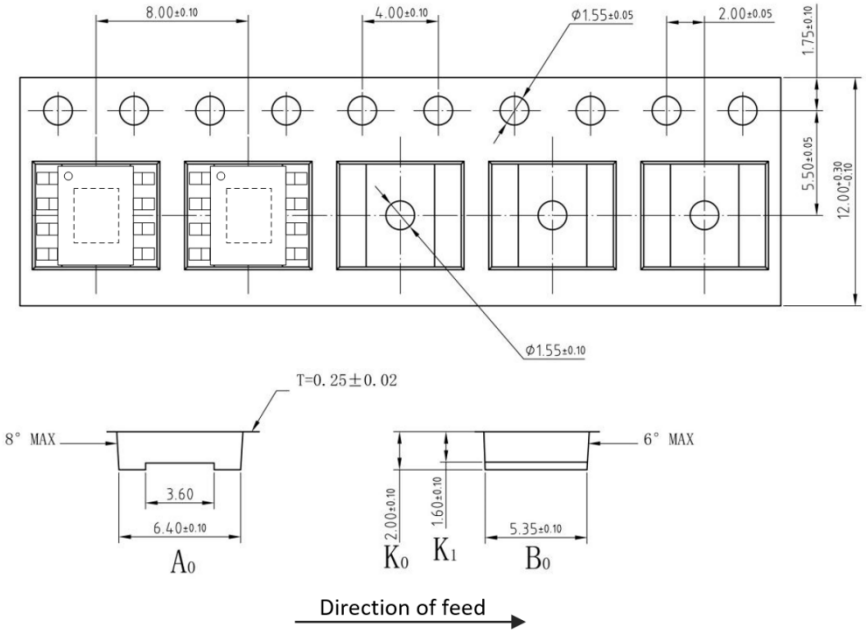
Symbol	Dimensions In Millimeters		Symbol	Dimensions In Millimeters	
	Min	Max		Min	Max
A	4.70	5.10	C	1.35	1.75
B	3.70	4.10	a	0.35	0.49
L	5.80	6.40	R	0.30	0.60
E	1.27 BSC		P	0°	7°
K	0.02	0.15	b	0.40	1.25
A1	3.1	3.5	B1	2.2	2.6

Figure 7. ESOP-8 Package Description

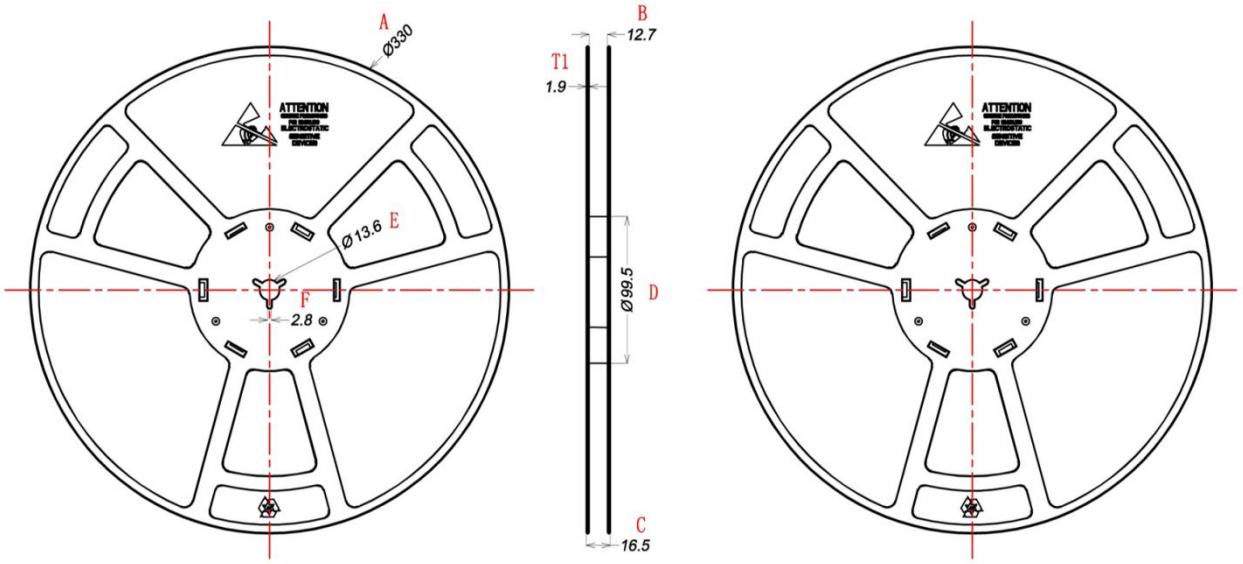
NOTE:

1. CONTROL DIMENSION ARE IN MILLIMETERS.
2. PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3. PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5. DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6. DRAWING IS NOT TO SCALE.

TAPE AND REEL INFORMATION



REEL DIMENSIONS



A	B	C	D	E	F	T1
Ø 330±1	12.7±0.5	16.5±0.3	Ø 99.5±0.5	Ø 13.6±0.2	2.8±0.2	1.9±0.2

Figure 8. ESOP-8 Tape and Reel Information

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. QUANTITY OF UNITS PER REEL IS 4000.
3. MSL LEVEL IS LEVEL 3.