Description

The ECP5702 is a Power Delivery (PD)SINK controller IC. The ECP5702 can request the maximum or specified voltage from the power supplies that complied with the Type-C PD protocol. The ECP5702 built in pull-low resistor onCC1 and CC2 pins. When the ECP5702 connected to the TYPE-C source device, the PD communication will be triggered and started automatically. The selected voltage will be requested and all related PD protocol will be completed. In the case of Vbus continuous power supply, you can change the TP voltage, change the protocol, and obtain the voltage required by the user. The voltage that can be obtained through the PD protocol: 5V/9V/12V/15V/20V.

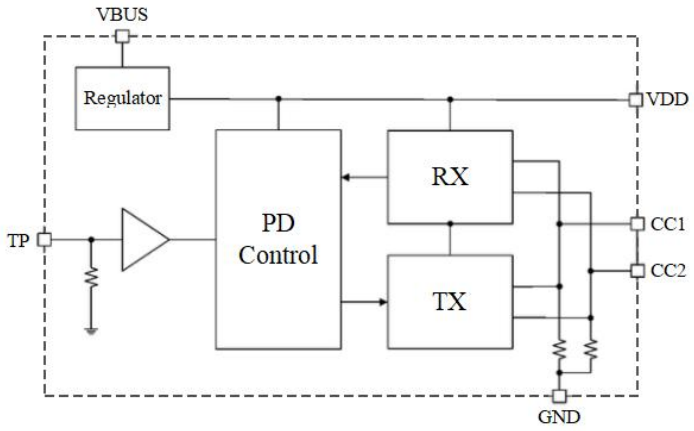
Feature

- Input voltage range : 4.6V~28V
- Support USB Type-C Specification Release 1.3
- Support USB PD2.0 and PD3.0 communication protocol up to seven power object
- Dynamic Vbus control
- Available voltage : 5V/9V/12V/15V/20V
- Package Type : SOT23-6L

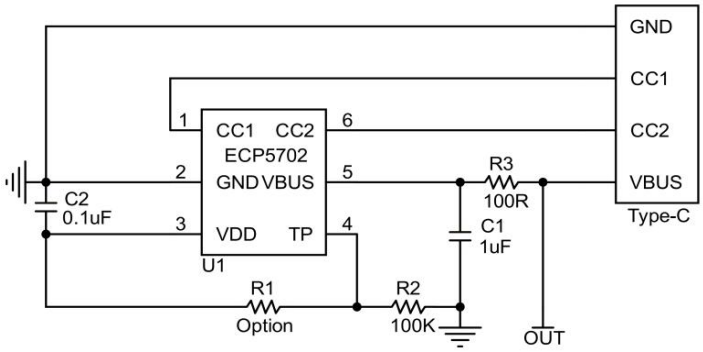
Application

- Battery Device
- NoteBook / MID / AIO
- Network
- DC-Motor
- Consumer /Home Application
- Lighting

Functional Block Diagram



Typical Application



Absolute Maximum Ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	VBUS		0		28	V
CC1 CC2 Voltage	VCC1 VCC2		-0.3		28	V
VDD TP Voltage	V_{VDD} V_{TP}		-0.3		3.3	V
Thermal Resistance	θ_{JA}	SOT23-6L			220	°C/W
Allowable Power Dissipation	PD	SOT23-6L TA≦+25° C			455	mW
Operation Temperature	T_{OP}		-25		+85	°C
Storage Temperature	T_{ST}	SOT23-6L	-40		+150	°C
Lead Temperature		soldering time 10sec			+260	°C

DC Electrical Characteristics

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Input Voltage Range	VBUS		4.6		20	V
VDD Regulator		VBUS = 5V		3.3		V
VDD Regulator Drive Current		VBUS = 5V			10	mA
Operation Current		VBUS = 5V		0.9		mA
Option Voltage(≤20V)(Max)		VBUS = 5V	20/24* VDD	21/24* VDD	VDD	V
Option Voltage(≤15V)		VBUS = 5V	16/24* VDD	17/24* VDD	18/24* VDD	V
Option Voltage(≤12V)		VBUS = 5V	12/24* VDD	13/24* VDD	14/24* VDD	V
Option Voltage(≤9V)		VBUS = 5V	8/24* VDD	9/24* VDD	10/24* VDD	V
Option Voltage(≤5V)		VBUS = 5V	0	5/24* VDD	6/24* VDD	V

PD Electrical Characteristics

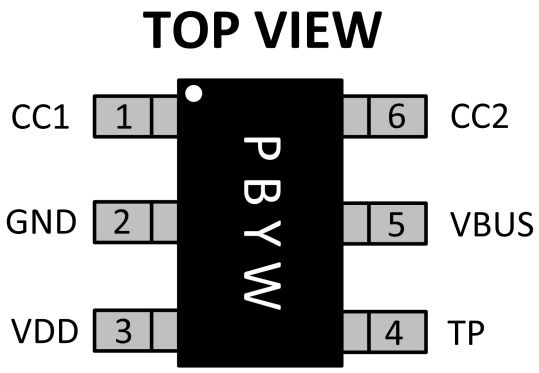
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Pull-down resistance through each C_CC pin when in a disconnect state	RD_CC		4.85	5.1	5.35	kΩ
Threshold Voltage of the pull-down FET in series with RD during dead battery	VTH_DB		0.5	0.9	1.2	V
PD data bit rate	PD_BITRAET		270	300	330	Kbps
Unit interval (1/PD_BITRATE)	UI		3.03	3.33	3.7	us
Capacitance for a cable plug (each plug on a cable may have up 25 pF to this value)	CCBLPLUG				25	pF
Cable characteristic impedance	ZCABLE		32		65	Ω
Receiver capacitance. Capacitance looking into C_CCn pin when in receiver mode	CRECEIVER		70		120	pF
TX Transmit Peak Voltage	VTXP		1.14	1.2	1.26	V
TX output impedance. Source output impedance at the Nyquist frequency of USB2.0 low speed (750kHz) while the source is driving the C_CCn line	ZDRIVER		33		75	Ω
Rise Time. 10% to 90% amplitude points, minimum is under an unloaded condition. Maximum set by TX mask	TRISE		300			ns
Fall Time. 90% to 10% amplitude points, minimum is under an unloaded condition. Maximum set by TX mask	TFALL		300			ns
Rx Receive Rising Input threshold	VRXTR		605	630	655	mV
Rx Receive Falling Input threshold	VRXTF		450	470	490	mV
Receiver input impedance	ZBMCRX		10			MΩ
Rx bandwidth limiting filter. Time constant of a single pole filter to limit broadband noise ingression	TRXFILTER		100			ns

Ordering Information

Part Number*	Package	Top Marking	MOQ
ECP5702	SOT23-6L	PBYW	3000EA/REEL

Package Reference

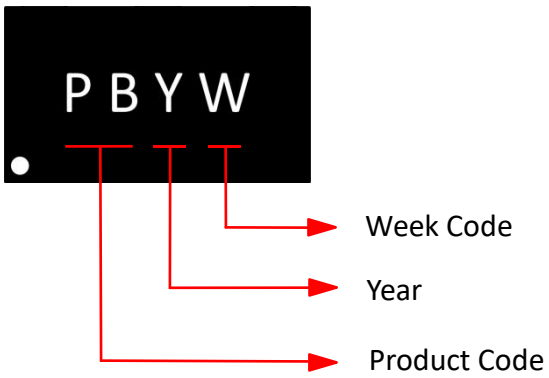
SOT23-6L



Pin#	Name	Description
1	CC1	PD CC1 pin
2	GND	Ground pin
3	VDD	Regulator output
4	TP	Test and option pin
5	VBUS	PD VBUS input pin
6	CC2	PD CC2 pin

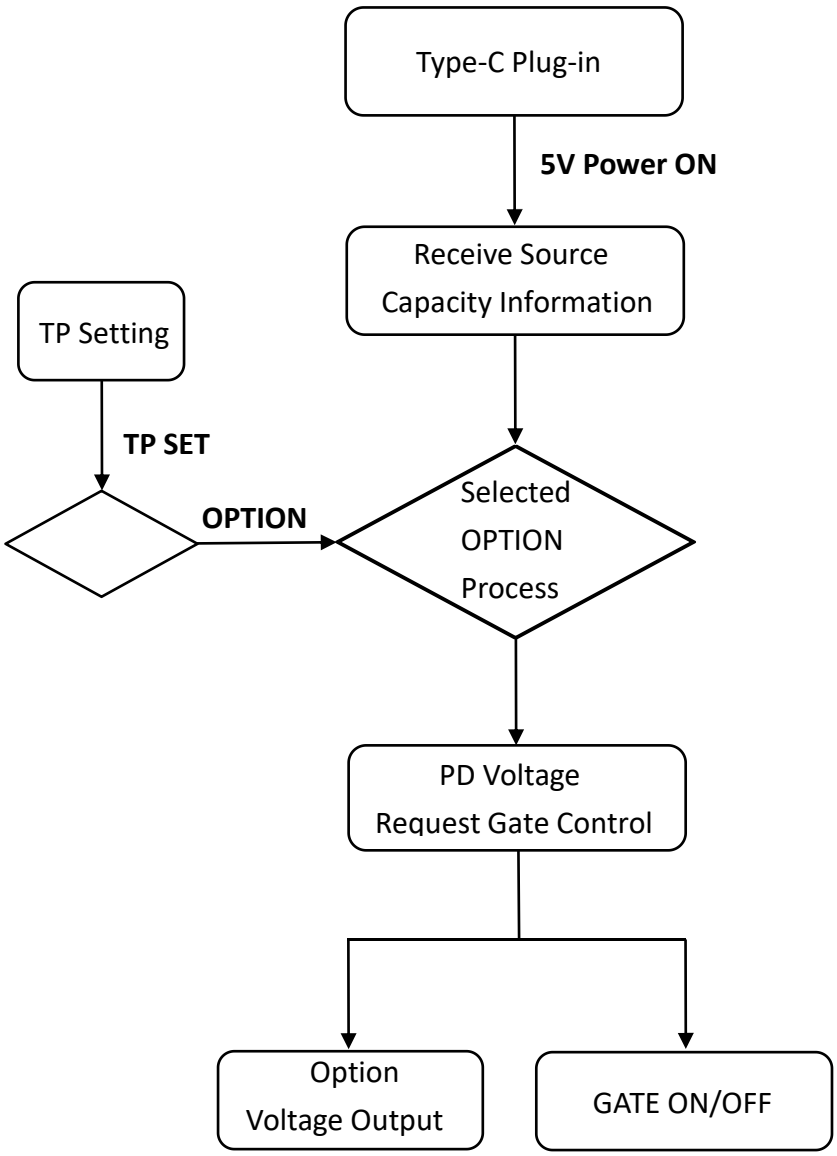
MarkLing Information

SOT23-6L



Operation Algorithm

The ECP5702 will complete the PD protocol negotiation after PD source device connected. The following diagram shows the PD connection algorithm.



Option Voltage Selection

ECP5702 can use the voltage on the TP pin to adjust the PD SINK protocol and this voltage adjustment can be dynamic. ECP5702 bases on the built-in voltage comparator to separate the TP input voltage into 5 options. The TP voltage can be adjusted by the dividing resistors from the VDD power, directly voltage setup from the MCU DAC output, or the MCU PWM output plus voltage filter Figure6. The relation between TP voltage and the PD SINK protocol voltage.

Option#	TP Voltage	PD Request	Description
OPT5	2.88V（21/24*VDD）	20V(Max)	Request Maximum Voltage of the Source Device
OPT4	2.34V（17/24*VDD）	15V	Request Voltage must ⩽15V
OPT3	1.79V（13/24*VDD）	12V	Request Voltage must ⩽12V
OPT2	1.24V（9/24*VDD）	9V	Request Voltage must ⩽9V
OPT1	0.69V（5/24*VDD）	5V	Request Voltage must ⩽5V

Resistor Selection for Common Output Voltages.

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
20	16	100
15	43	100
12	86	100
9	170	100
5	390/NC	100

The option selection of ECP5702 is used to protect the connected device.The following example shows the result of requested voltage.

Source Power (W)	PD Source Supply						ECP5702 Request Voltage				
	Object 28V	Object 20V	Object 15V	Object 12V	Object 9V	Object 5V	Option 1	Option 2	Option 3	Option 4	Option 5
140	√	√	√		√	√	5	9	9	15	20
100		√	√	√	√	√	5	9	12	15	20
98		√	√		√	√	5	9	9	15	20
60		√	√	√	√	√	5	9	12	15	20
45		√	√	√	√	√	5	9	12	15	20
35		√	√		√	√	5	9	9	15	20
20					√	√	5	9	9	9	9
15 (PD)						√	5	5	5	5	5

Typical Application Circuit

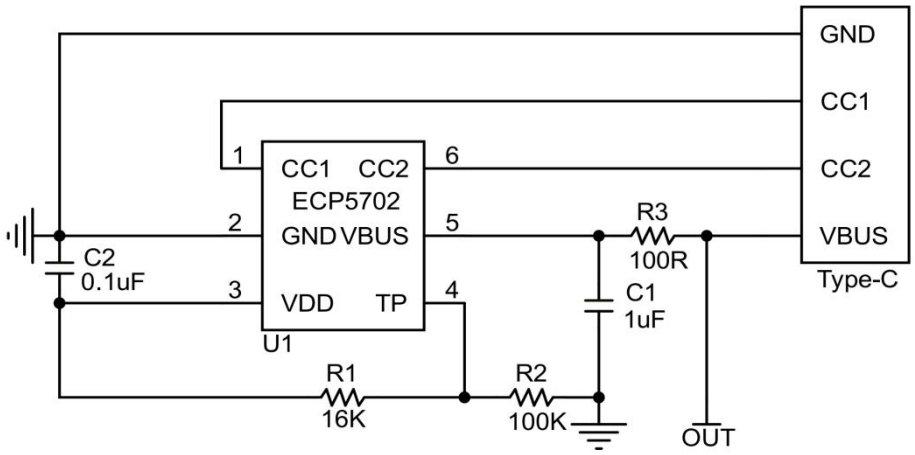


Figure 1: 20V Output Typical Application Circuit

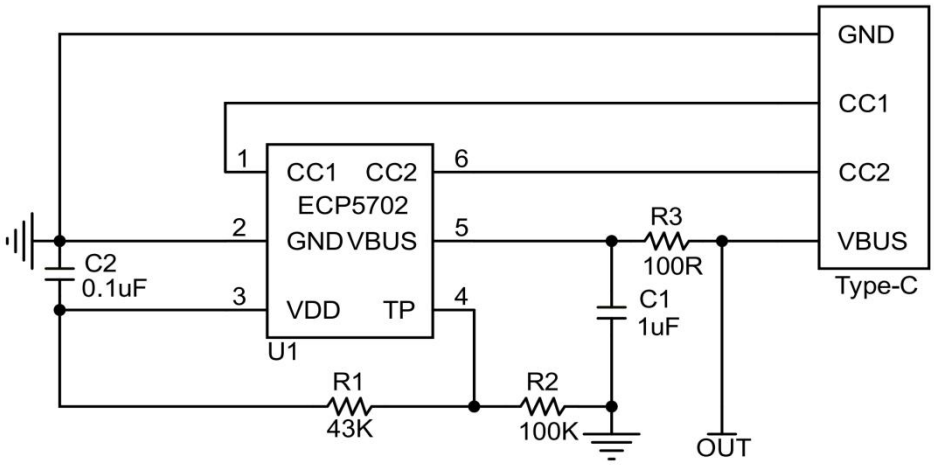


Figure 2: 15V Output Typical Application Circuit

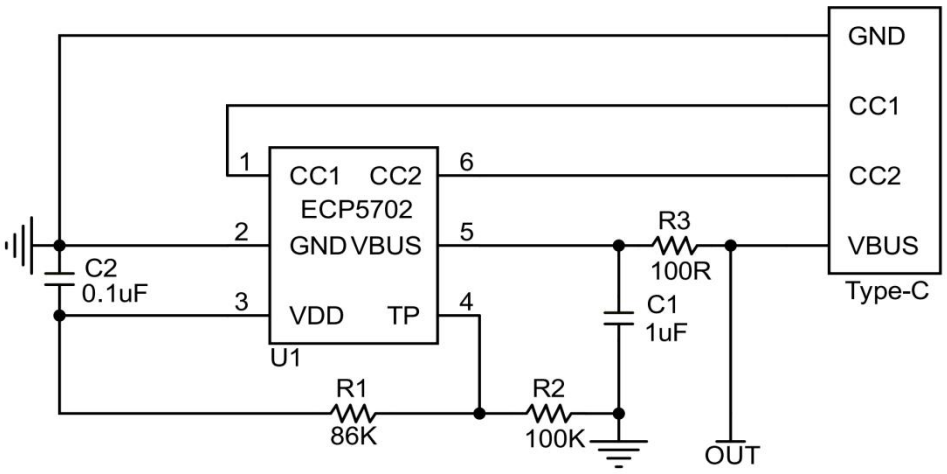


Figure 3: 12V Output Typical Application Circuit

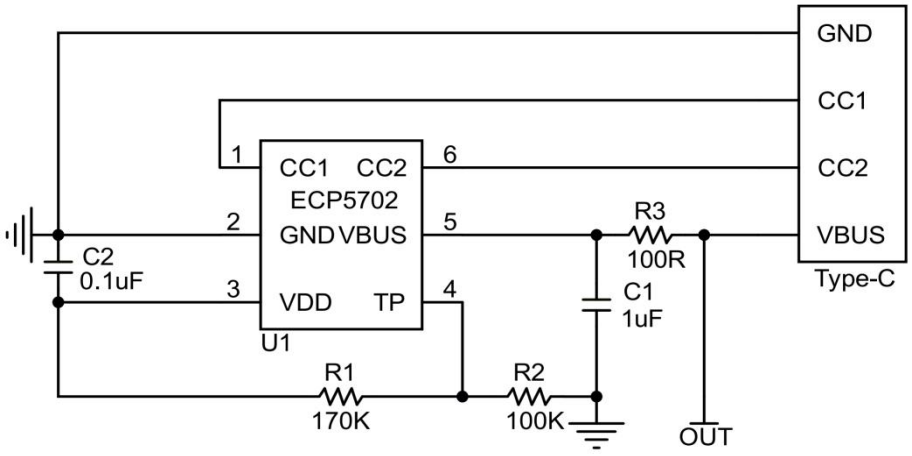


Figure 4: 9V Output Typical Application Circuit

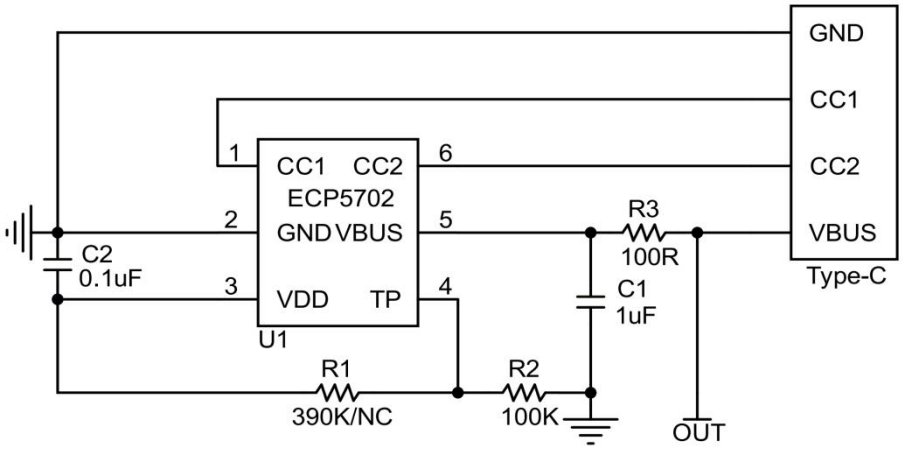


Figure 5: 5V Output Typical Application Circuit

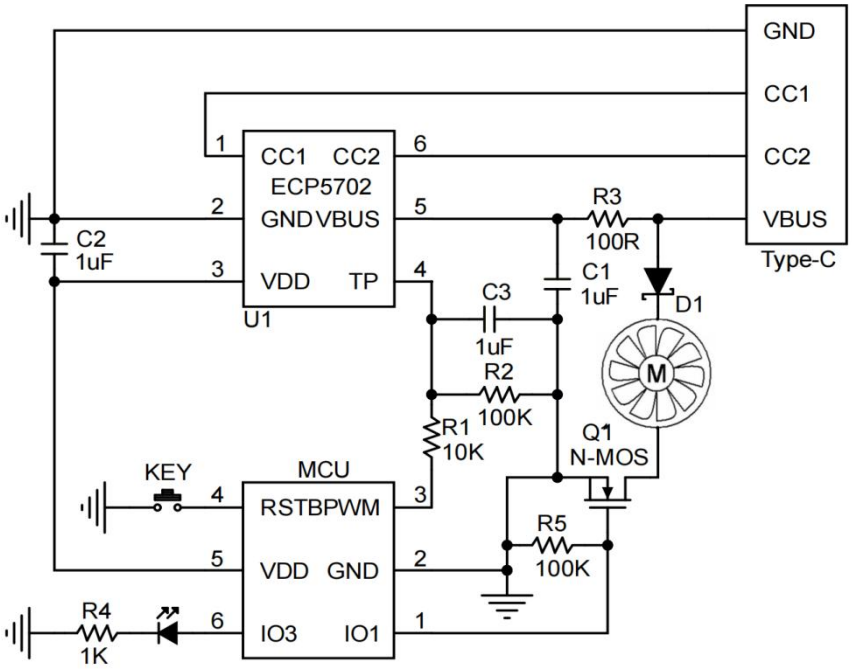
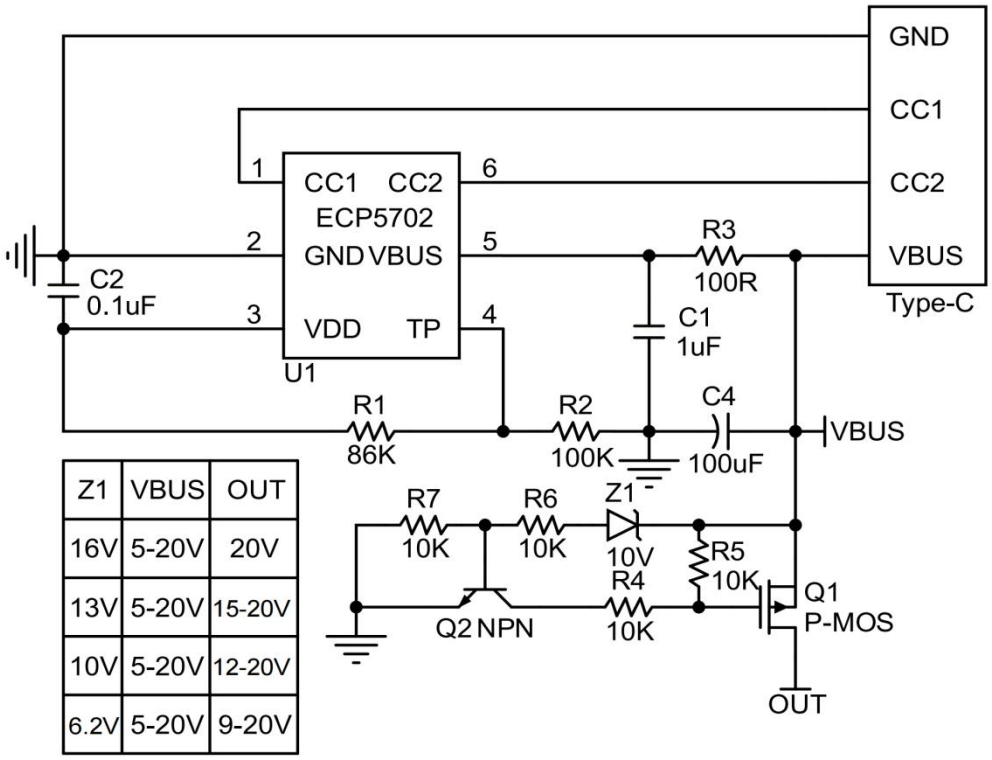


Figure 6:MCU Control Application Circuit

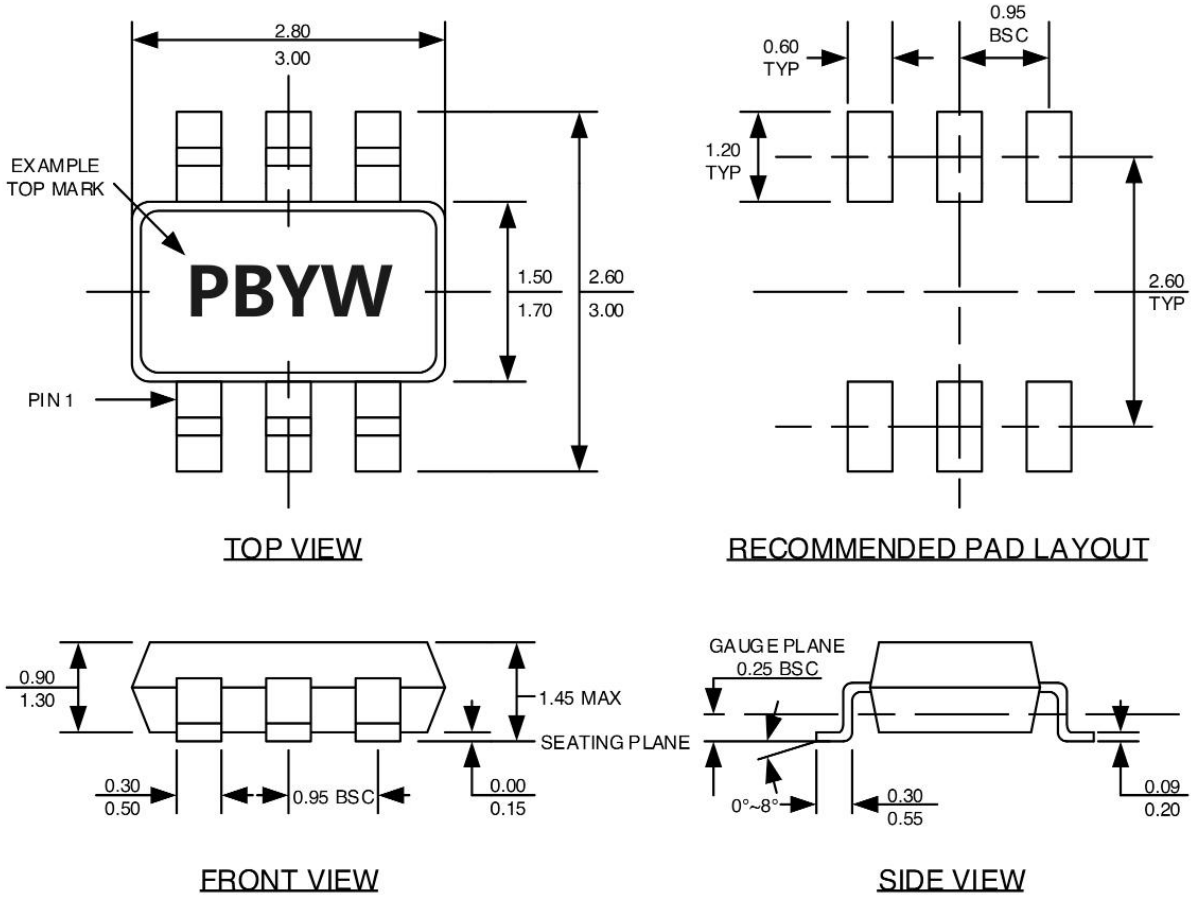


Z1	VBUS	OUT
16V	5-20V	20V
13V	5-20V	15-20V
10V	5-20V	12-20V
6.2V	5-20V	9-20V

Figure 7: Set Up The Start Voltage Control Application Circuit

Package Outline

SOT23-6L



Note:

1. All dimensions are in millimeters.
2. Package length does not include mold flash, protrusion or gate burr.
3. Package width does not include flash or protrusion.
4. Lead coplanarity (bottom of leads after forming) shall be 0.10 millimeters max.
5. Pin 1 is lower left pin when reading top mark from left to right.