55V,2μA I_Q,350mA Low-Dropout Linear Voltage Regulator

Description

The XR9200 series is a high voltage，ultralow-power，low dropout voltage regulator. The device can deliver 350mA output current with a dropout voltage of 350mV and allows an input voltage as high as 55V. The typical quiescent current is only 2μA. The device is available in fixed output voltages of 1.8,2.5,2.8,3.0,3.3,3.6 and 5.0V.The device features integrated short-circuit and thermal shutdown protection.Although designed primarily as fixed voltage regulators, the device can be used with external components to obtain variable voltages.

Features

- Wide Input Voltage Range: 3.0V to 55V
- Low Power Consumption: 2 μA (Typ)
- Maximum Output Current: 350mA
- Low Dropout Voltage:
  V_{DROP} = 35mV @I_{OUT} = 10mA (Typ.)
  V_{DROP} = 350mV @I_{OUT} = 100mA (Typ.)
- High PSRR: 85dB @1kHz
- Output Voltage Accurate: ± 2 %
  (±1 % It needs to be customized)
- Excellent Line/Load Regulation
- Good Transient Response
- Integrated Short-Circuit Protection
- Over-Temperature Protection
- Output Current Limit
- Low Temperature Coefficient
- Stable with Ceramic Capacitor
- RoHS Compliant and Lead (Pb) Free
- -40°C to +85°C Operating Temperature Range
- Fixed Output Voltage Versions: 1.8,2.5,2.8,3.0,3.3,3.6 and 5.0V.
- Available in Green SOT23-3, SOT89-3 Packages

Applications

- Powering MCUs and CAN/LIN transceivers
- Battery-powered equipment
- EV and HEV battery management systems
- Portable, Battery Powered Equipment
- Car Audio/Video Equipmen
- Body control modules

Application Circuits

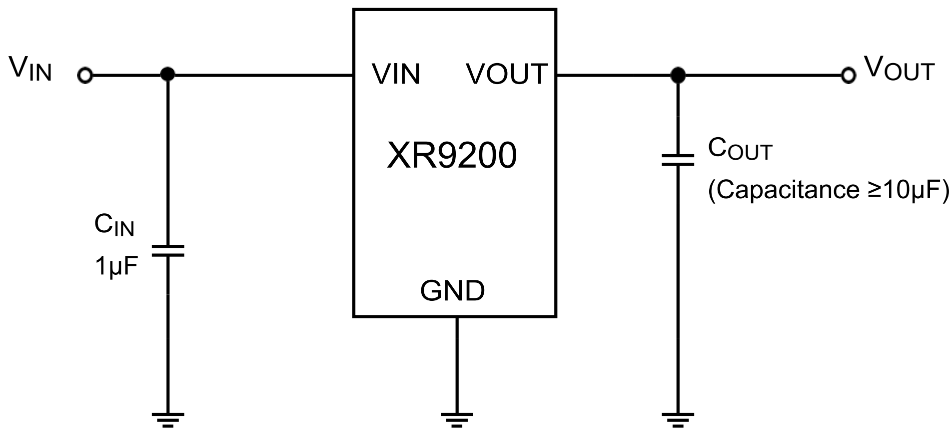
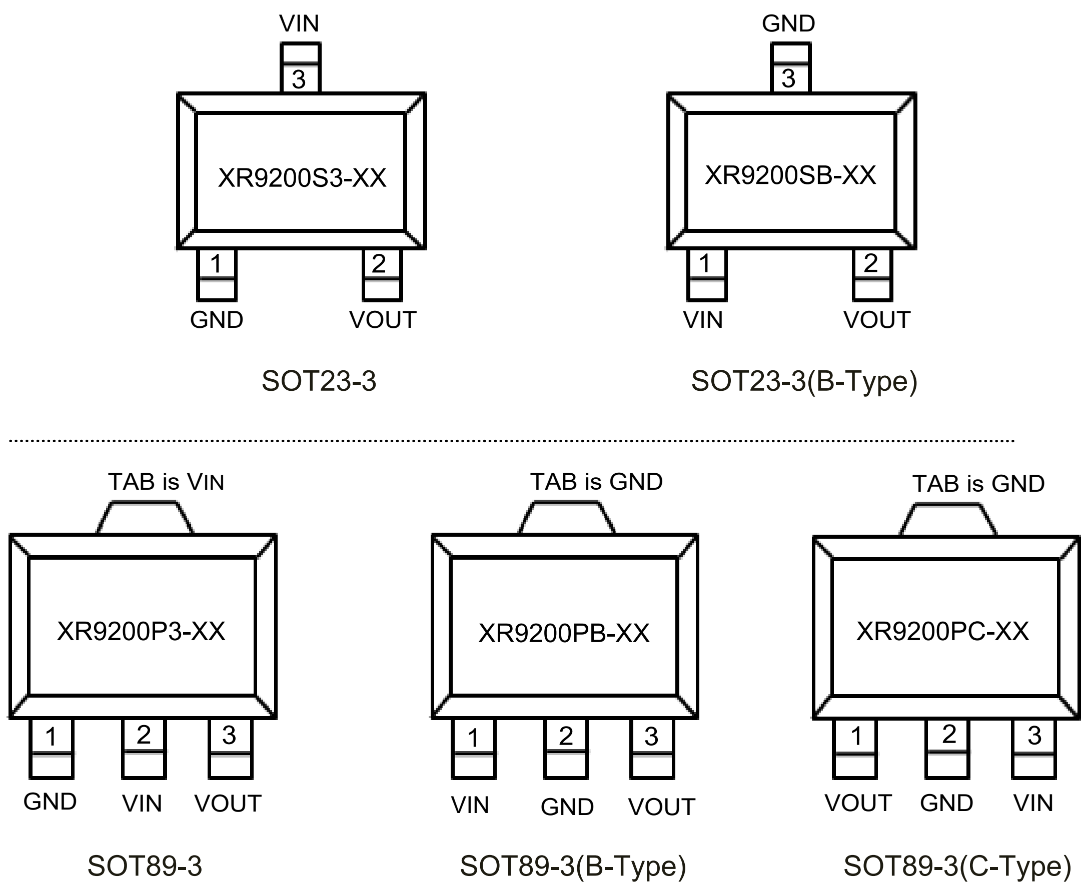


Figure 1. XR9200 Typical Application Circuit

Pin Configuration (TOP VIEW)



Pin Description

Pin No.					Pin Name	Pin Function
SOT23-3		SOT89-3				
S3	SB	P3	PB	PC		
1	3	1	2	2	GND	Ground
3	1	2	1	3	VIN	Power Input
2	2	3	3	1	VOUT	Output Voltage
TAB	In PCB layout, prefer to use large copper area to cover this pad for better thermal dissipation					

Order Information

XR9200①②-③④

Designator	Symbol	Description
①②	S3 , SB , P3 , PB , PC	SOT23-3, SOT23-3B, SOT89-3, SOT89-3B, SOT89-3C
③④	Integer e.g 1.8=18	Output Voltage 1.8,2.5,2.8,3.0,3.3,3.6 and 5.0V.

Part NO.	Marking	Description	Package	T/R Qty
XR9200S3-XX	-----	XR9200 55V,2μA I_Q,350mA Low-Dropout Linear Voltage Regulator	SOT23-3	3,000 PCS
XR9200SB-XX	-----		SOT23-3(B-Type)	3,000 PCS
XR9200P3-XX	-----		SOT89-3	1,000 PCS
XR9200PB-XX	-----		SOT89-3(B-Type)	1,000 PCS
XR9200PC-XX	-----		SOT89-3(C-Type)	1,000 PCS

For marking information, contact our sales representative directly

All AISIS parts are Pb-Free and adhere to the RoHS directive.

Absolute Maximum Ratings

Item		Symbol	Rating	Unit
Supply Input Voltage		V_{IN}	-0.3 ~ 60	V
V_{OUT} to V_{IN}		V_{OUT} _ V_{IN}	-35 ~ -0.3	V
Regulated Output Voltage		V_{OUT}	-0.3 ~ 6.0	V
Output Current		I_{OUT}	Internally limited	mA
Power Dissipation P_D @T_A=+25℃	SOT23-3	P_D	500	mW
	SOT23-3(B-Type)		500	
	SOT89-3		750	
	SOT89-3(B-Type)		1250	
	SOT89-3(C-Type)		1250	
Thermal Resistance (Junction to air)	SOT23-3	$θ_{JA}$	250	°C /W
	SOT23-3		250	
	SOT89-3		165	
	SOT89-3(B-Type)		100	
	SOT89-3(C-Type)		100	
Human Body Model (HBM)		±4000		V
Charged Device Mode (CDM)		±2000		V
Machine Mode (MM)		200		V
Storage Temperature Range		T_{STG}	-65 ~ +150	°C
Operating Junction Temperature		T_J	+150	°C
Lead Temperature (Soldering 10s)		T_{LEAD}	+260	°C

Note：

1、Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute-maximum-rated conditions for extended period may affect device reliability.

2、Ratings apply to ambient temperature at +25°C

3、The package thermal impedance is calculated in accordance to JESD 51-7.

Recommended Operating Conditions

Item	Min	Max	Unit
Operating Ambient Temperature	-40	+85	°C
Input Voltage	3.0	45	V
Output Voltage	1.8	5.0	V

Electronic Characteristics

Test Conditions: V_{IN} = V_{OUT} +2V,C_{IN}=1uF,C_{OUT} =10uF,T_A=25℃,unless otherwise specifi

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage	——	3.0	——	55	V
I_Q	Quiescent Current	V_{IN} = 12V, No Load	—	2	5	μA
V_{OUT}	Output Voltage	V_{IN} = 12V I_{OUT} = 10mA	V_{OUT} x 0.98	——	V_{OUT} x 1.02	V
I_{OUT}	Output Current	——	——	350	——	mA
V_{DROP}	Dropout Voltage	I_{OUT} = 10mA V_{OUT} = V_{OUTNOM} – 0.1V	——	35	75	mV
		I_{OUT} = 100mA V_{OUT} = V_{OUTNOM} – 0.1V	——	350	500	mV
		I_{OUT} = 350mA V_{OUT} = V_{OUTNOM} – 0.1V	——	1200	1400	mV
Δ V_{LOAD}	Load Regulation	V_{IN} = 12V 1mA ≤ I_{OUT} ≤ 100mA	——	0.02	0.025	%/mA
Δ V_{LINE}	Line Regulation	V_{OUTNOM} + 2V ≤ V_{IN} ≤ 45V I_{OUT} = 1mA	——	0.01	0.02	%/V
I_{LIMIT}	Current Limit	——	——	500	——	mA
T_{OTSD}	Thermal Shutdown Temperature	——	——	+150	——	°C
T_{HYOTSD}	Thermal Shutdown Hysteresis	——	——	+20	——	°C
PSRR	Power Supply Rejection Ratio	V_{IN} = 12V, I_{OUT} = 10mA V_{OUT} = 3.3V @1kHz	——	85	——	dB
Von	Output Noise Voltage	C_{OUT} =10uF, I_{OUT} =30mA BW = 10Hz~100kHz	—	100	—	μVrms

Note : All limits specified at room temperature (TA = 25°C) unless otherwise specified. All room temperature limits are 100% production tested. All limits at temperature extremes are ensured through correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Functional Block Diagram

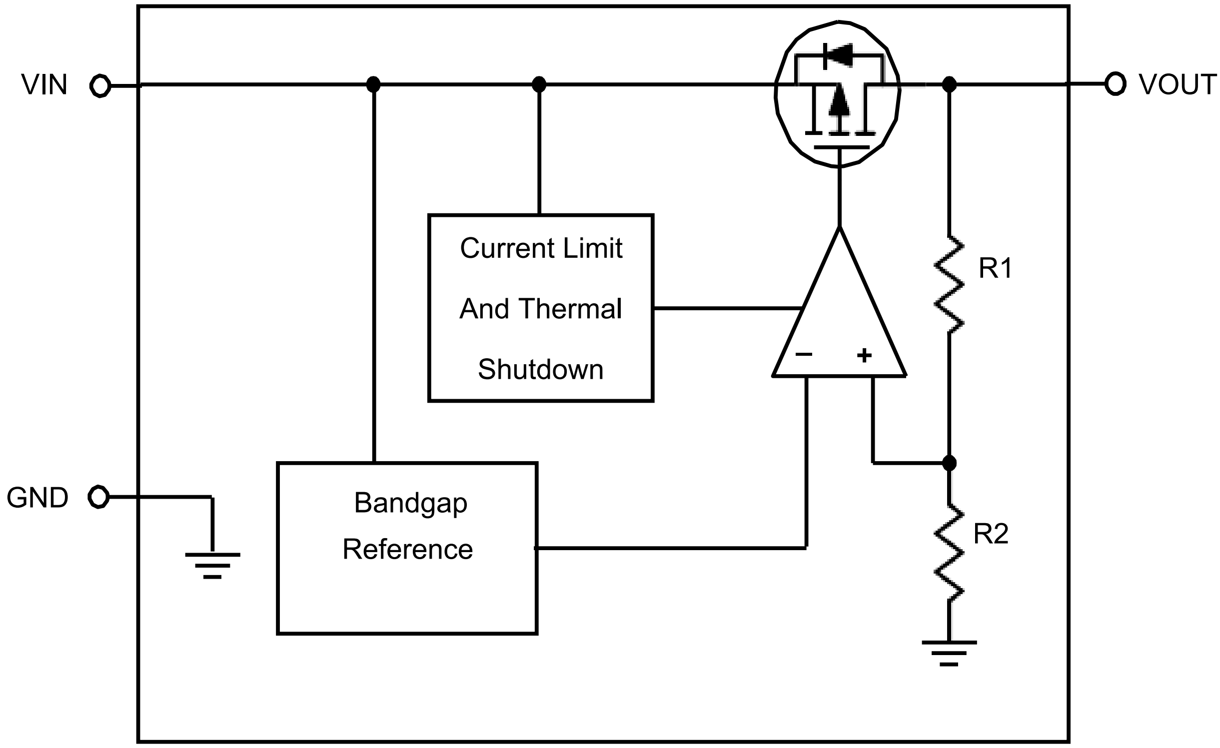


Figure 2. XR9200 Block Diagram

Application Guideline

■ Input Capacitor

A ≥ 1μF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

■ Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended output capacitance is ≥10μF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to VOUT and GND pins.

■ Dropout Voltage

The dropout voltage refers to the voltage difference between the VIN and VOUT pins while operating at specific output current. The dropout voltage V_{DROP} also can be expressed as the voltage drop on the pass-FET at specific output current (I_{RATED}) while the pass-FET is fully operating at ohmic region and the pass-FET can be characterized asan resistance RDS(ON). Thus the dropout voltage can bedefined as ($V_{DROP} = V_{IN} - V_{OUT} = R_{DS(ON)} \times I_{RATED}$). Fornormal operation, the suggested LDO operating range is ($V_{IN} > V_{OUT} + V_{DROP}$) for good transient response and PSRR ability. Vice versa, while operating at the ohmic region will degrade the performance severely.

■ Thermal Application

For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below:

T_A=25°C, AISIS DEMO PCB,

The max $P_D = (T_j - T_A) / \theta_{JA}$.

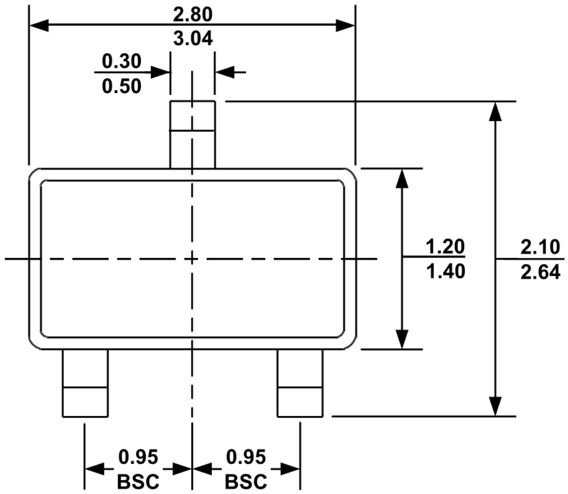
Power dissipation (P_D) is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:

$P_D = (V_{IN} – V_{OUT}) \times I_{OUT}$

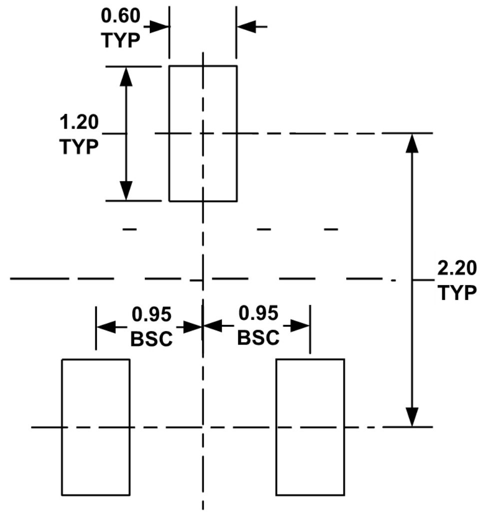
■ Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the XR9200 ground pin using as wide and as short of a copper trace as is practical.Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

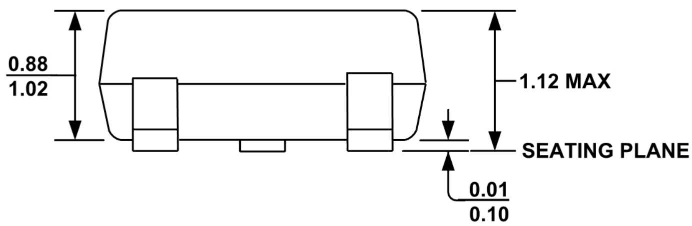
PACKAGE OUTLINE DRAWING FOR SOT23-3



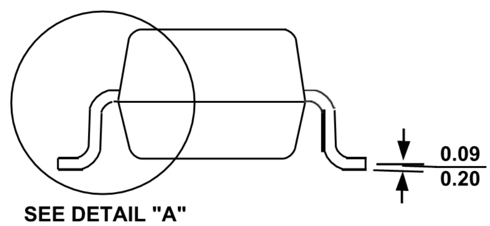
TOP VIEW



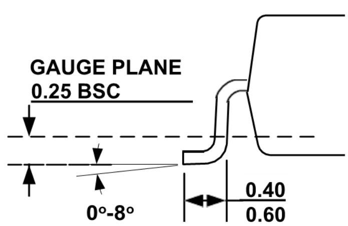
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

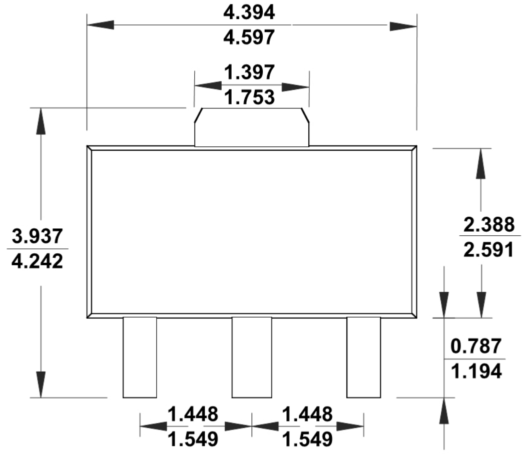


DETAIL “A”

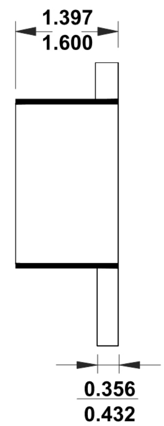
NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING IS NOT TO SCALE.
6) PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK FROM LEFT TO RIGHT, (SEE EXAMPLE TOP MARK)
7) DRAWING CONFORMS TO JEDEC TO-236, VARIATION AB.

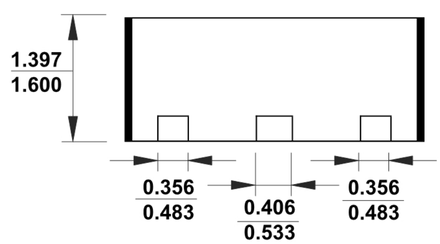
PACKAGE OUTLINE DRAWING FOR SOT89-3



TOP VIEW



SIDE VIEW



FRONT VIEW

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