HX2305

-20V P-Channel Enhancement Mode MOSFET

■ *DESCRIPTION*

The 2305 is the P-Channel logic enhancement mode power field effect transistor is produced using high cell density advanced trench technology..

This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application, and low in-line power loss are needed in a very small outline surface mount package.

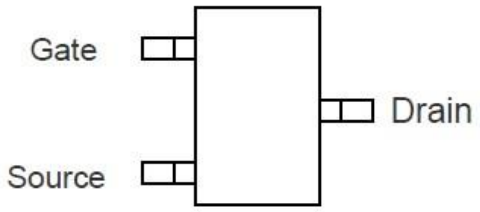
■ *FEATURE*

- ***-20V/-4.3A, $R_{DS(ON)}$=30mΩ (typ.)@V_{GS}=-4.5V***
- ***-20V/-3.5A,$R_{DS(ON)}$=40mΩ (typ.)@V_{GS}=-2.5V***
- ***-20V/-2.0A,$R_{DS(ON)}$=56mΩ (typ.)@V_{GS}=-1.8V***
- ***-20V/-1.0A,$R_{DS(ON)}$=85mΩ (typ.)@V_{GS}=-1.5V***
- Super high design for extremely low $R_{DS(ON)}$
- Exceptional on-resistance and Maximum DC current capability
- Full RoHS compliance
- SOT23-3L package design

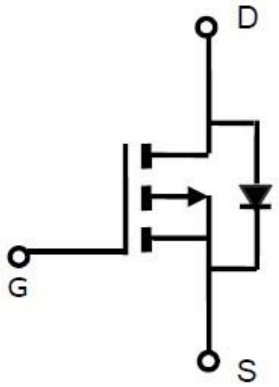
■ *APPLICATIONS*

- Power Management
- Portable Equipment
- DC/DC Converter
- Load Switch
- DSC
- LCD Display inverter

■ *PIN CONFIGURATION*



TOP VIEW
SOT-23



P-Channel

■ PART NUMBER INFORMATION

2305A-BB C	A= Package Code S: SOT BB=Handing Code TR: Tape&Reel C=Lead Plating Code G: Green Product

■ ORDERING INFROMATION

Part Number	Package Code	Package	Shipping
2305AS-TRG	**S**	SOT23-3L	**3000EA / T&R**

※ Year Code : 0~9

※ Week Code : A~Z(1-26); a~z(27~52)

※ G : Green Product. This product is RoHS compliant.

■ ABSOLUTE MAXIMUM RATINGS (T_A = 25℃ Unless otherwise noted)

Symbol	Parameter		Typical	Unit
V_{DSS}	Drain-Source Voltage		-20	V
V_{GSS}	Gate-Source Voltage		±10	V
I_D	Continuous Drain Current (T_C=25℃)	V_{GS}=-10V	-4.2	A
	Continuous Drain Current (T_C=70℃)		-3.5	A
I_{DM}	Pulsed Drain Current		-20	A
P_D	Power Dissipation	T_A=25℃	1.5	W
		T_A=70℃	0.9	
T_J	Operation Junction Temperature		150	℃
T_{STG}	Storage Temperature Range		-55~+150	℃
$R_{\theta JA}$	Thermal Resistance Junction to Ambient		120	℃/W

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress rating only and functional device operation is not implied

■ *ELECTRICAL CHARACTERISTICS(T_A=25℃ Unless otherwise noted)*

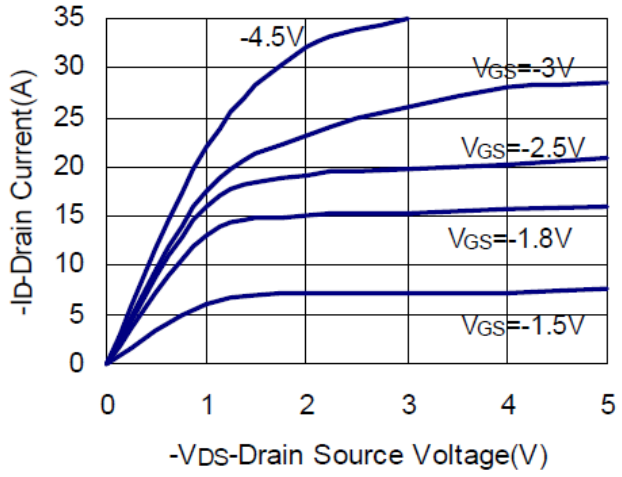
Symbol	Parameter	Condition	Min	Typ	Max	Unit
Static Parameters						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	V_{GS}=0V, I_D=-250uA	-20			V
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS}, I_D=-250uA	-0.3		-1.0	V
I_{GSS}	Gate Leakage Current	V_{DS}=0V, V_{GS}=±10V			±100	nA
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=-20V, V_{GS}=0			-1	uA
		V_{DS}=-20V, V_{GS}=0 T_J=55℃			-5	
$R_{DS(ON)}$	Drain-Source On-Resistance	V_{GS}=-4.5V, I_D=-4.0A		30	40	mΩ
		V_{GS}=-2.5V, I_D=-4.0A		40	60	
		V_{GS}=-1.8V, I_D=-2.0A		56	78	
		V_{GS}=-1.5V, I_D=-1.0A		85	110	
Gfs	Forward Transconductance	V_{DS}=-5V, I_D=-4.0A		22		S
Source-Drain Diode						
V_{SD}	Diode Forward Voltage	I_S=-1.0A, V_{GS}=0V		-0.67	-1.2	V
Dynamic Parameters						
Q_g	Total Gate Charge	V_{DS}=-10V V_{GS}=-4.5V I_D=-4.0A		11.1		nC
Q_{gs}	Gate-Source Charge			3.1		
Q_{gd}	Gate-Drain Charge			2.4		
C_{iss}	Input Capacitance	V_{DS}=-10V V_{GS}=0V f=1MHz		989		pF
C_{oss}	Output Capacitance			167		
C_{rss}	Reverse Transfer Capacitance			75.5		
$T_{d(on)}$	Turn-On Time	V_{DS}=-10V I_D=-3.7A V_{GEN}=-4.5V R_G=1Ω		712		nS
T_r				1386		
$T_{d(off)}$	Turn-Off Time			9.1		
T_f				4		

Note: 1. Pulse test: pulse width<=300uS, duty cycle<=2%

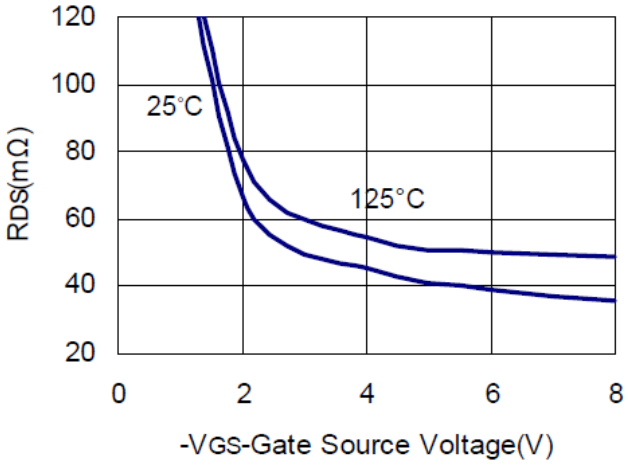
2.Static parameters are based on package level with recommended wire bonding

■ *TYPICAL CHARACTERISTICS (25℃ Unless Note)*

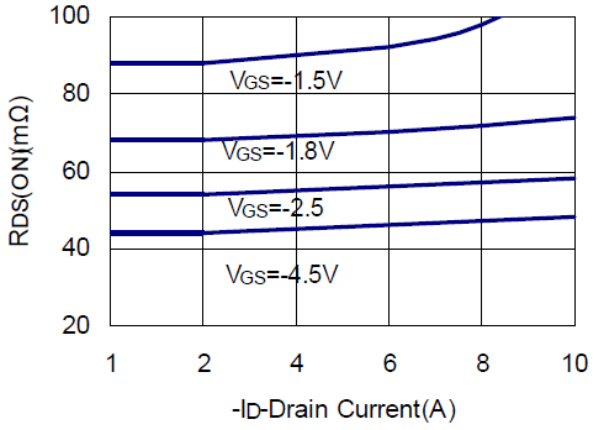
Output Characteristics



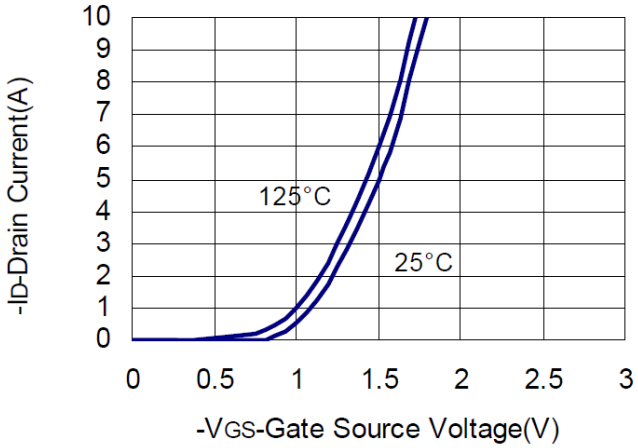
Drain-Source On Resistance



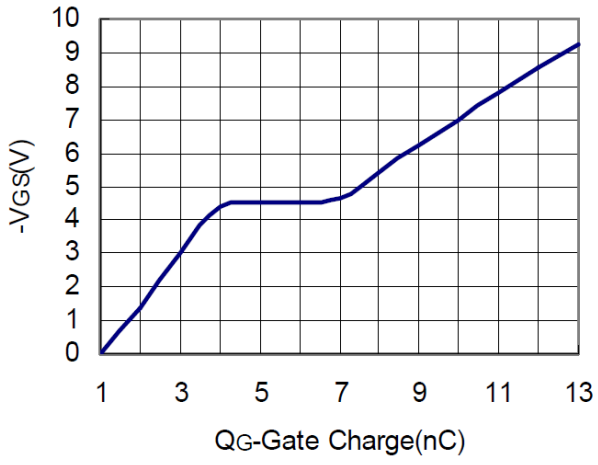
Drain Source On Resistance



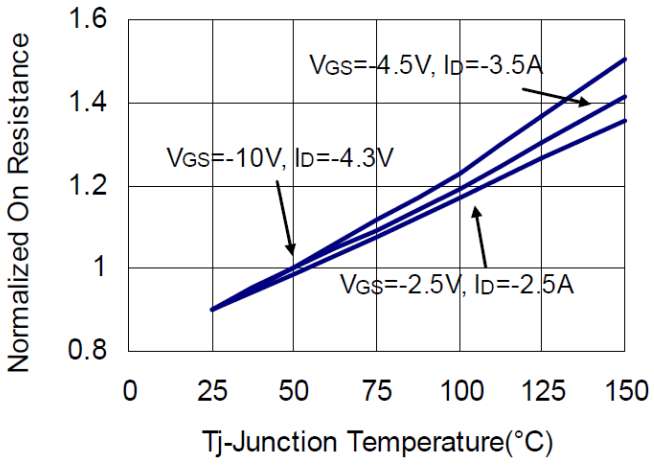
Transfer Characteristics



Gate Charge

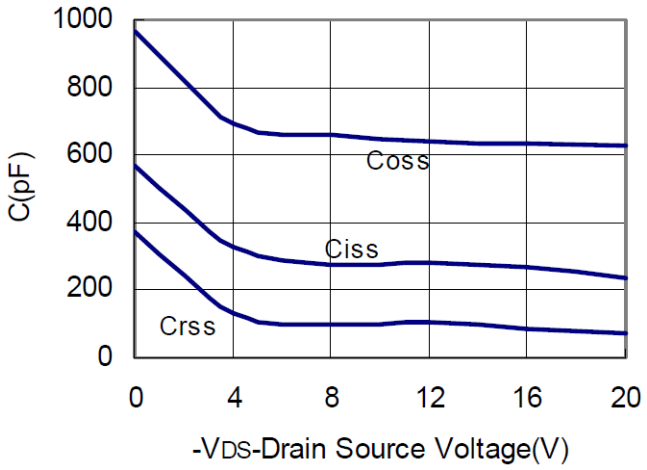


Drain Source Resistance

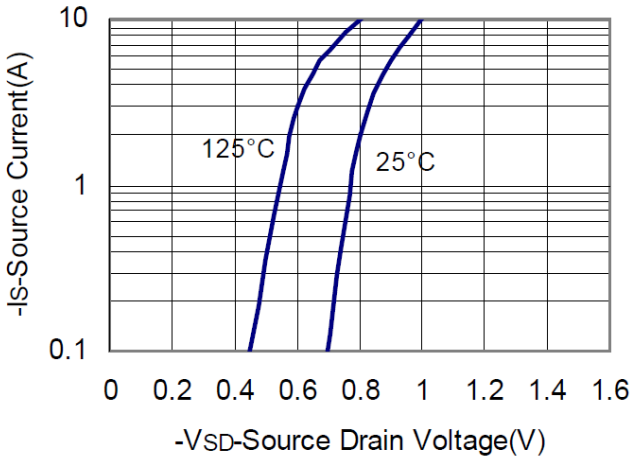


■ *TYPICAL CHARACTERISTICS (continuous)*

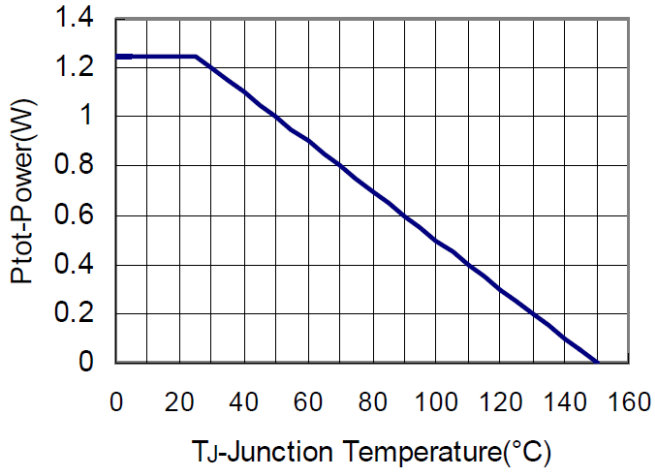
Capacitance



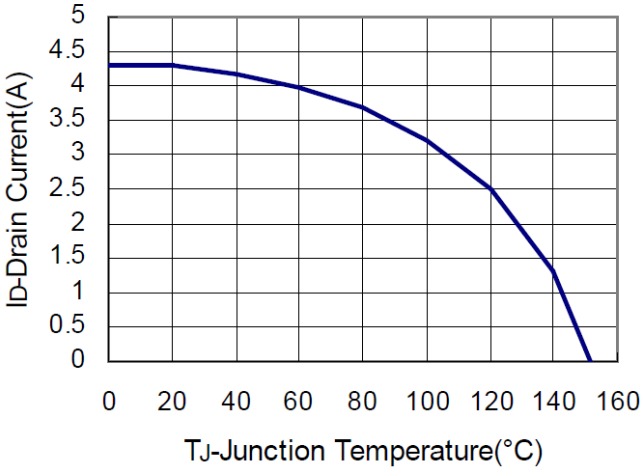
Source Drain Diode Forward



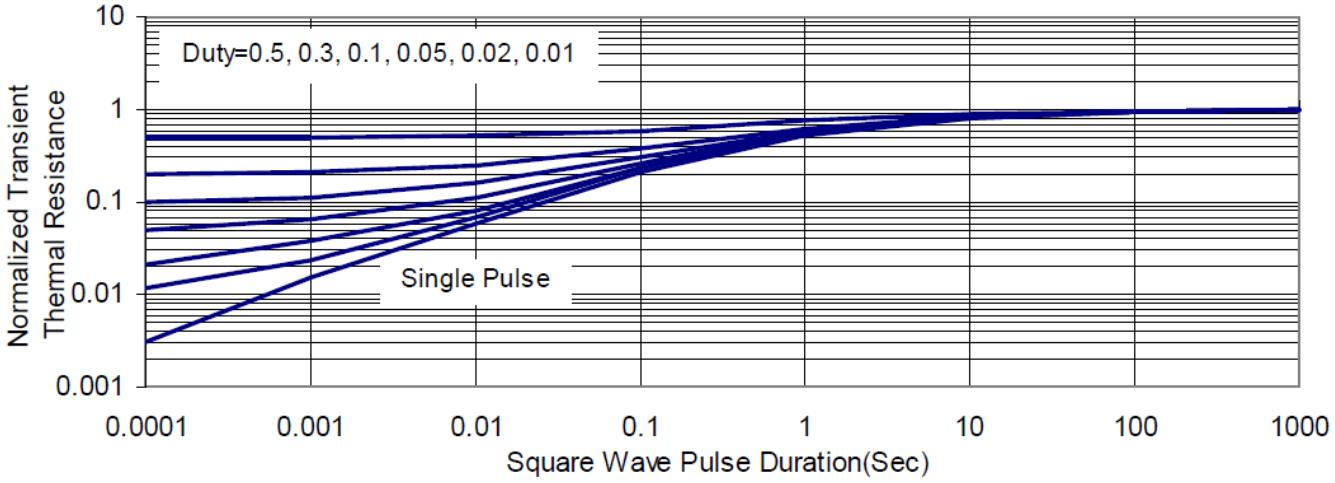
Power Dissipation



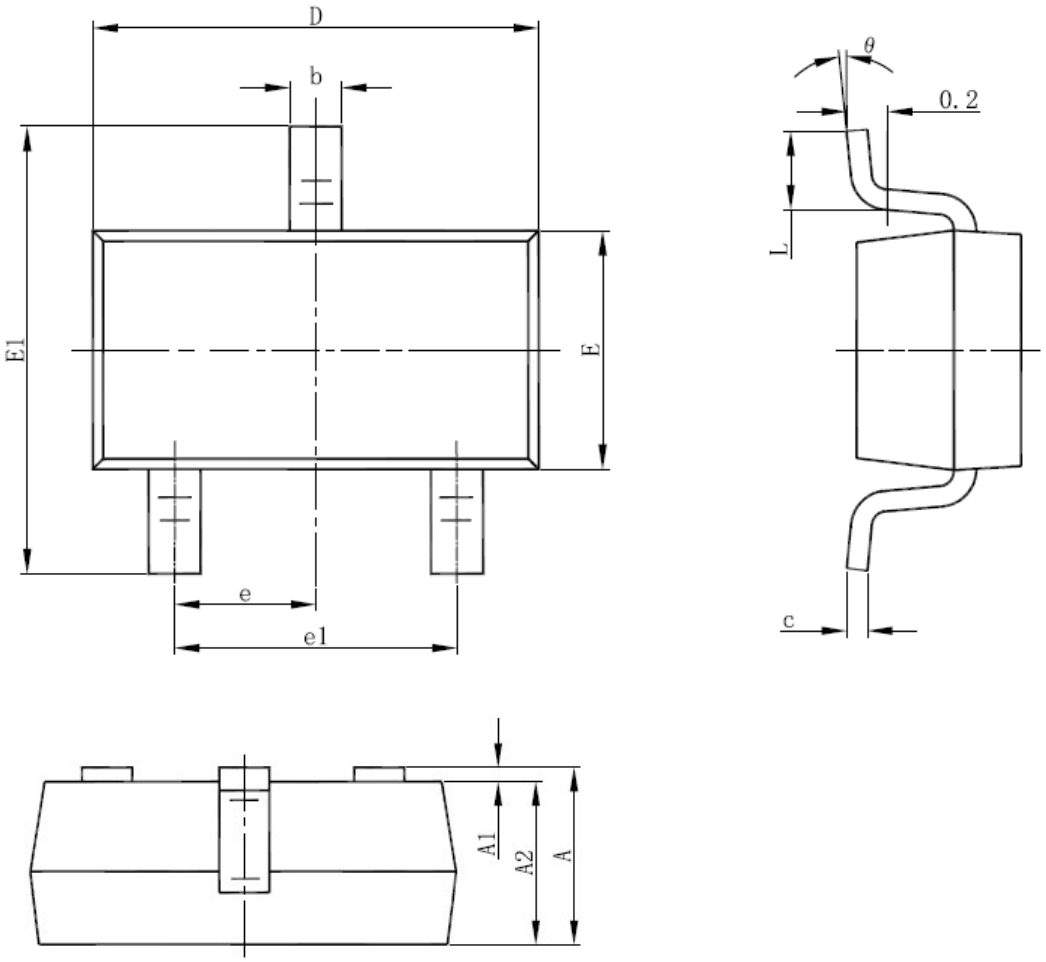
Drain Current



Thermal Transient Impedance



■ *SOT23-3L PACKAGE OUTLINE DIMENSIONS*

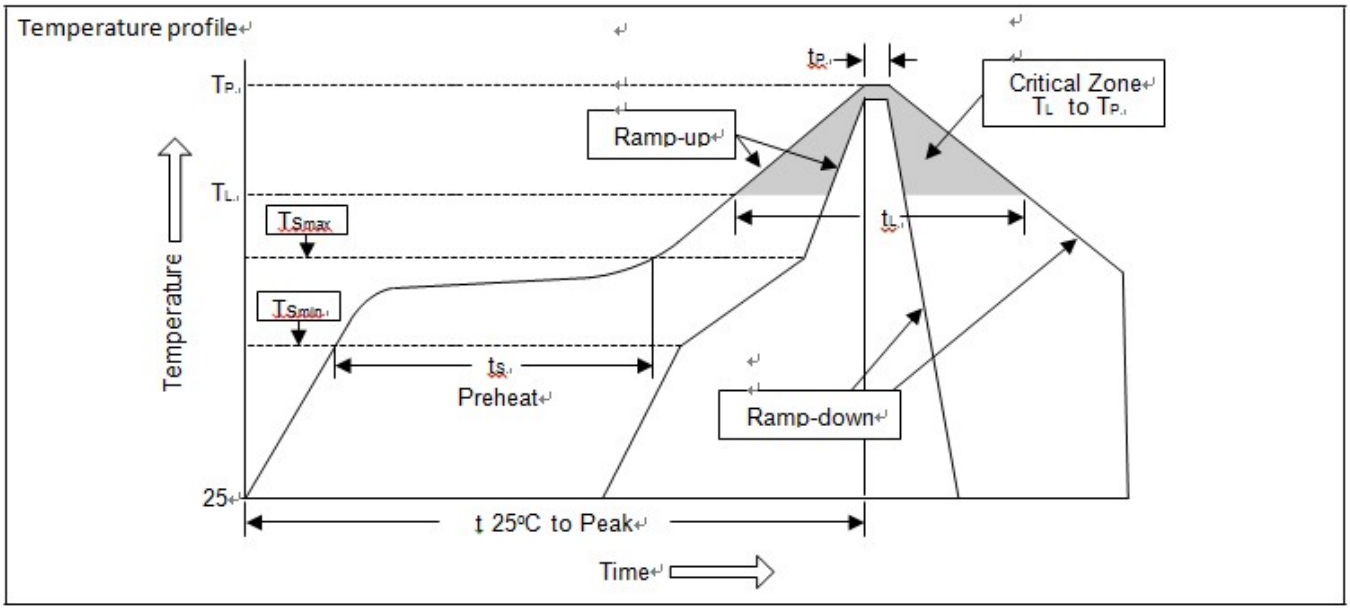


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.020	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950(BSC)		0.037(BSC)	
e1	1.800	2.000	0.071	0.079
L	0.300	0.600	0.012	0.024
θ	0°	8°	0°	8°

■ *SOLDERING METHODS FOR UNIVERCHIP*

Storage environment Temperature=10℃~35℃ Humidity=65%±15%

Reflow soldering of surface mount device



Profile Feature	Sn-Pb Eutectic Assembly	Pb free Assembly
Average ramp-up rate (T_L to T_P)	<3℃/sec	<3℃/sec
Preheat -Temperature Min (Ts_{min}) -Temperature Max (Ts_{max}) -Time (min to max) (ts)	 100℃ 150℃ 60~120 sec	 150℃ 200℃ 60~180 sec
Tsmax to T_L -Ramp-up Rate	<3℃/sec	<3℃/sec
Time maintained above -Temperature (T_L) -Time (t_L)	 183℃ 60~150 sec	 217℃ 60~150 sec
Peak Temperature (T_P)	240℃+0/-5℃	260℃+0/-5℃
Time within 5℃ of actual Peak Temperature (t_P)	10~30 sec	20~40 sec
Ramp-down Rate	<6℃/sec	<6℃/sec
Time 25℃ to Peak Temperature	<6 minutes	<6 minutes

Flow (wave) soldering (solder dipping)

Product	Peak Temperature	Dipping Time
Pb device	245℃±5℃	5sec±1sec
Pb-Free device	260℃+0/-5℃	5sec±1sec

This integrated circuit can be damaged by ESD UniverChip Corporation recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedure can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.