

## N-CHANNEL ENHANCEMENT MODE POWER MOSFET

# TF20N03

### Description

The TF20N03 TO-252 uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

### General Features

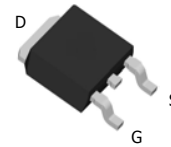
VDSS	RDS(ON) @10V (typ)	ID
30V	14 mΩ	20A

- High density cell design for ultra low Rdson
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

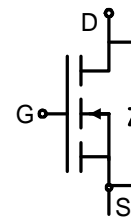
### Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply

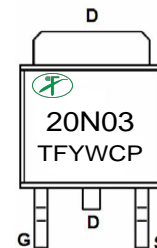
### TO-252



### Equivalent Circuit



### MARKING



Y :year code W :week code

### Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	30 V	
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	20	A
Drain Current-Pulsed <sup>(Note 1)</sup>	$I_{DM}$	50	A
Maximum Power Dissipation	$P_D$	30	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ\text{C}$

### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	3.5	$^\circ\text{C/W}$
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**N-CHANNEL ENHANCEMENT MODE POWER MOSFET**
**TF20N03**
**Electrical Characteristics (T<sub>A</sub>=25°C unless otherwise noted)**

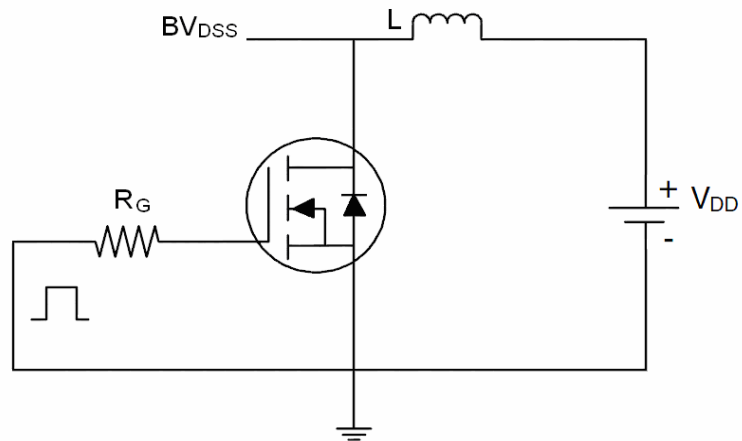
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	V <sub>GS</sub> =0V, I <sub>D</sub> =250μA	30	32	-	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> =28V, V <sub>GS</sub> =0V	-	-	500	nA
Gate-Body Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V	-	-	±100	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	1	1.45	2.0	V
Drain-Source On-State Resistance	R <sub>DS(on)</sub>	V <sub>GS</sub> =10V, I <sub>D</sub> =15 A		14	18	mΩ
		V <sub>GS</sub> =4.5V, I <sub>D</sub> =10A		18	26	
Forward Transconductance	g <sub>FS</sub>	V <sub>DS</sub> =5V, I <sub>D</sub> =10A		10		S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> =25V, V <sub>GS</sub> =0V, F=1.0MHz	-	1165	-	PF
Output Capacitance	C <sub>oss</sub>		-	142	-	PF
Reverse Transfer Capacitance	C <sub>rss</sub>		-	99	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> =20V, I <sub>D</sub> =1.0A V <sub>GS</sub> =10V, R <sub>G</sub> =6.0Ω	-	11.7	-	nS
Turn-on Rise Time	t <sub>r</sub>		-	5.2	-	nS
Turn-Off Delay Time	t <sub>d(off)</sub>		-	18	-	nS
Turn-Off Fall Time	t <sub>f</sub>		-	6.0	-	nS
Total Gate Charge	Q <sub>g</sub>	V <sub>DS</sub> =20V, I <sub>D</sub> =5A, V <sub>GS</sub> =10V	-	11	-	nC
Gate-Source Charge	Q <sub>gs</sub>		-	2.2	-	nC
Gate-Drain Charge	Q <sub>gd</sub>		-	4.2	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	V <sub>SD</sub>	V <sub>GS</sub> =0V, I <sub>S</sub> =20A	-	-	12	V
Diode Forward Current <sup>(Note 2)</sup>	I <sub>S</sub>		-	-	10	A

**Notes:**

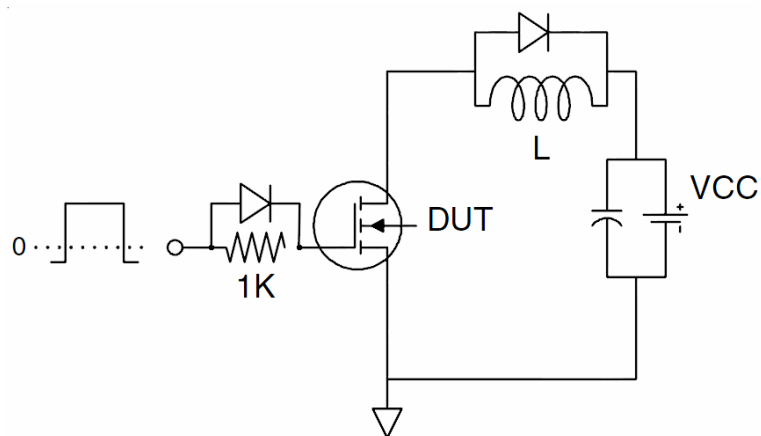
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production

## Test circuit

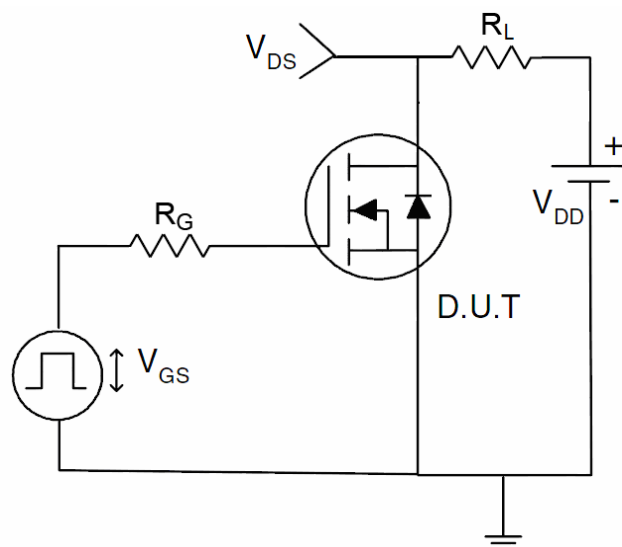
### 1) $E_{AS}$ test Circuits



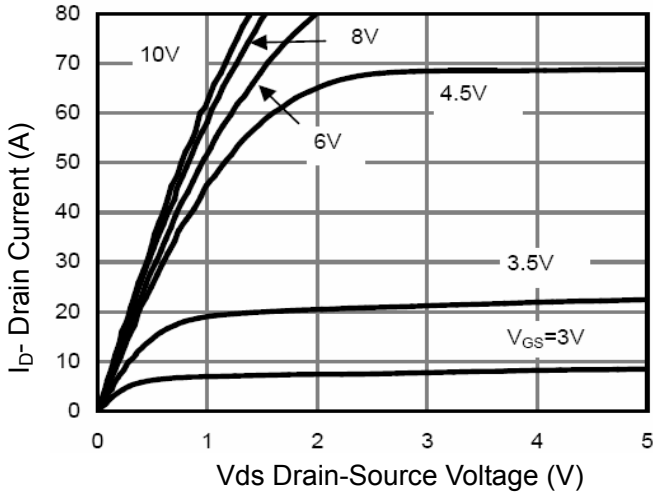
### 2) Gate charge test Circuit:



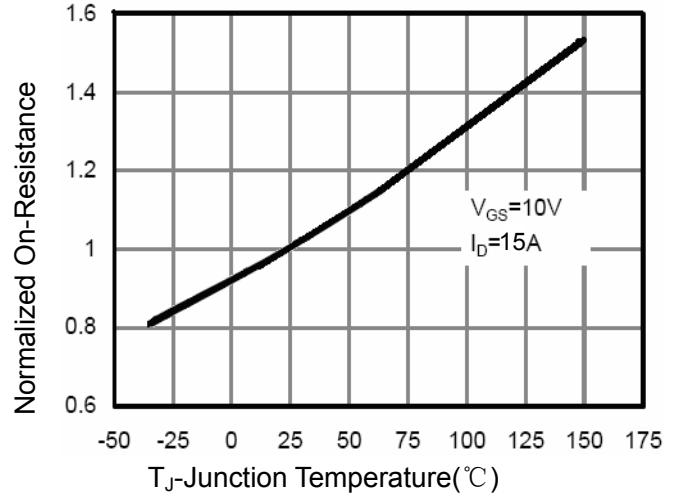
### 3) Switch Time Test Circuit:



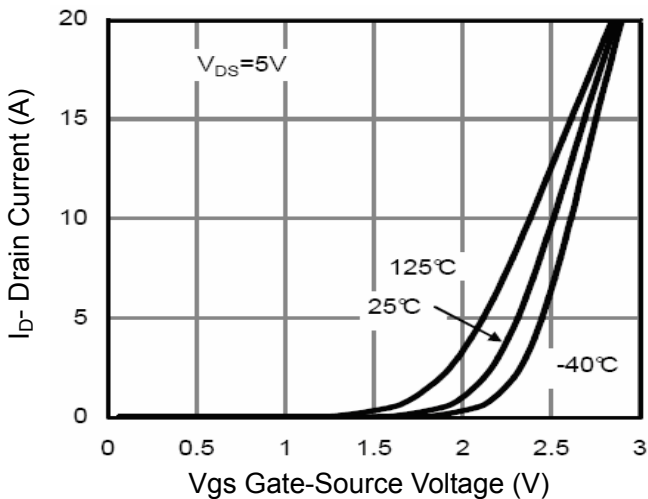
**Typical Electrical and Thermal Characteristics (Curves)**



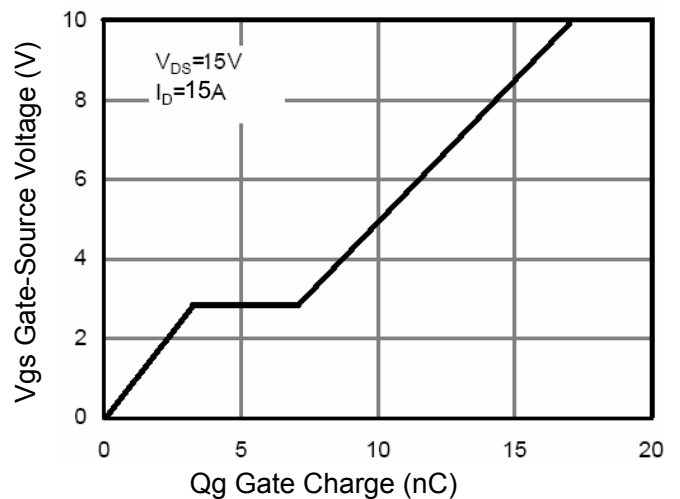
**Figure 1 Output Characteristics**



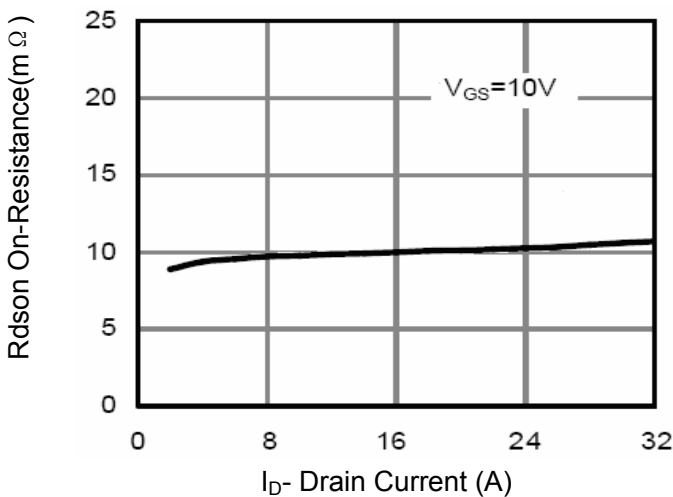
**Figure 4  $R_{dson}$ -Junction Temperature**



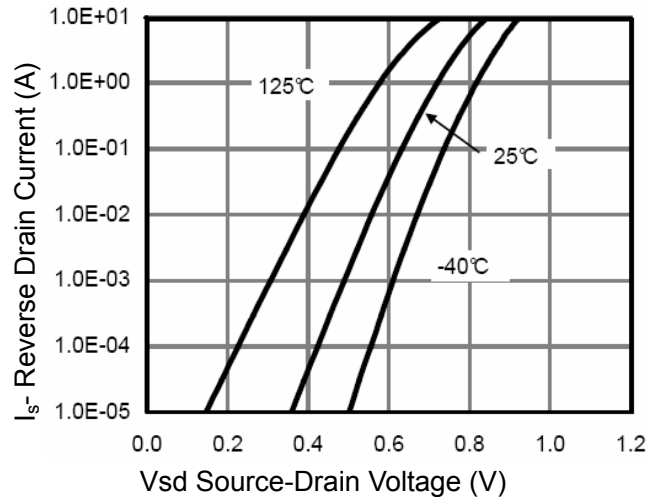
**Figure 2 Transfer Characteristics**



**Figure 5 Gate Charge**



**Figure 3  $R_{dson}$ - Drain Current**



**Figure 6 Source- Drain Diode Forward**

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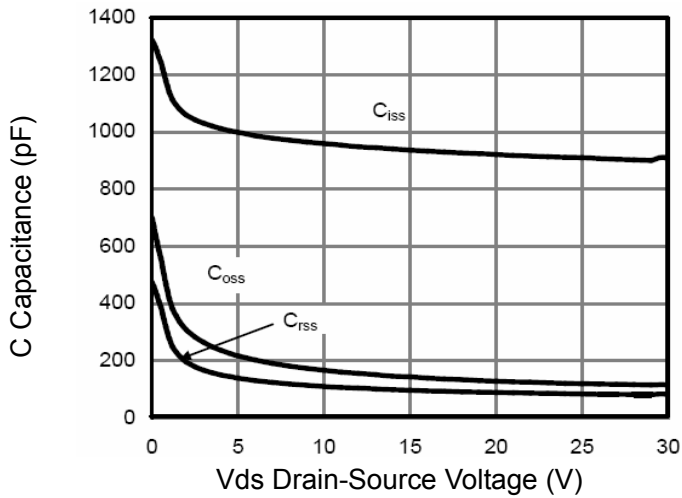


Figure 7 Capacitance vs Vds

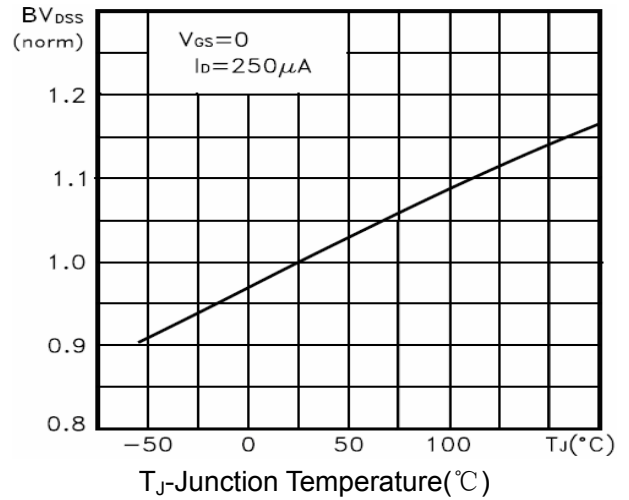


Figure 9  $BV_{DSS}$  vs Junction Temperature

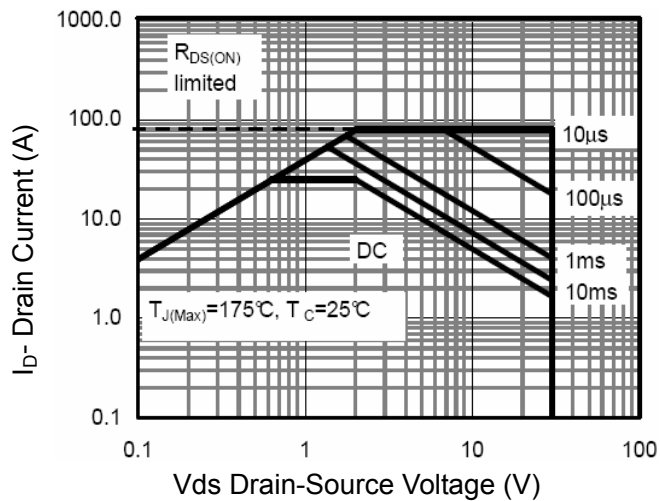


Figure 8 Safe Operation Area

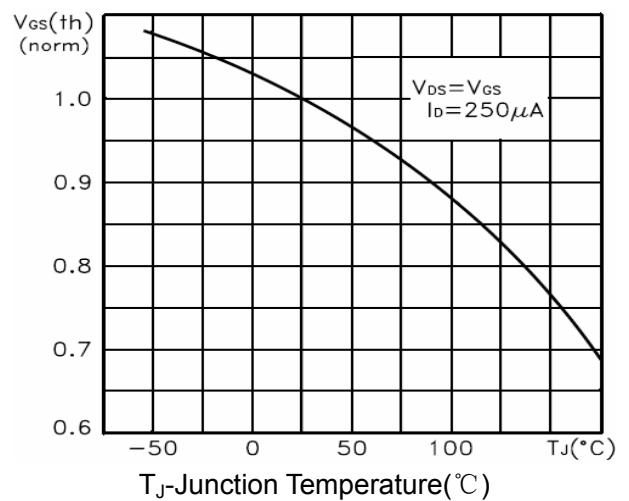


Figure 10  $V_{GS(th)}$  vs Junction Temperature

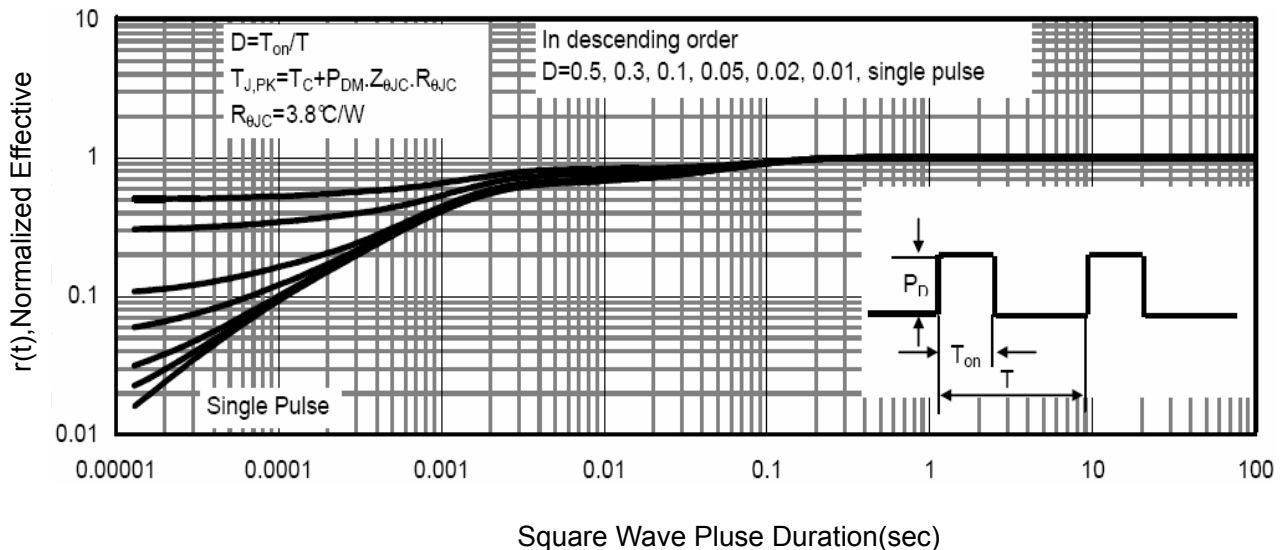
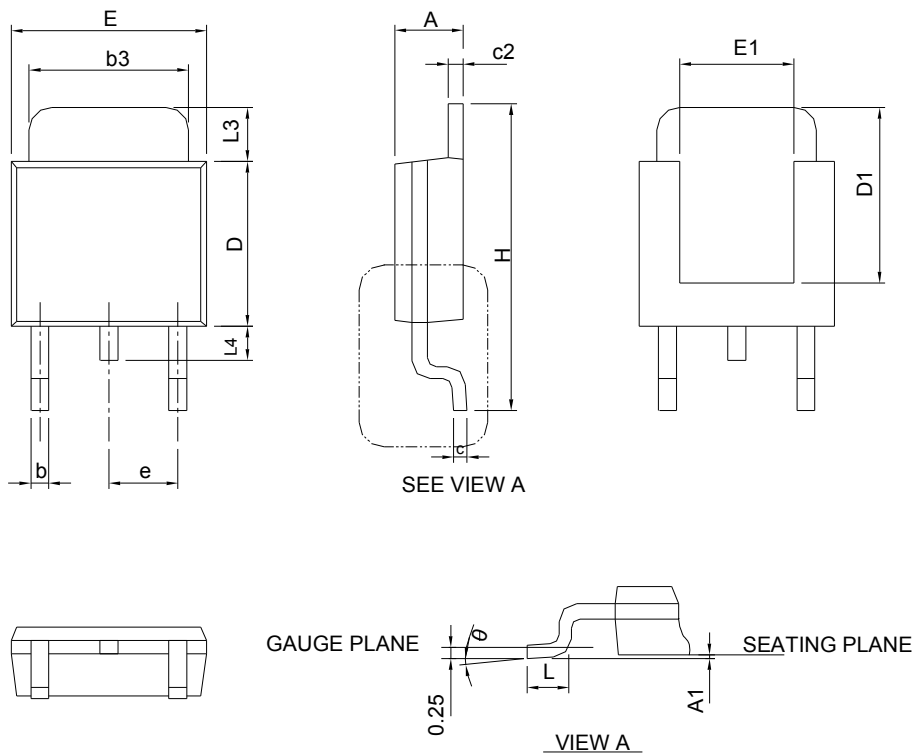


Figure 11 Normalized Maximum Transient Thermal Impedance

Package Information

TO-252-2L



SYMBOL	TO-252-3			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.39	0.086	0.094
A1		0.13		0.005
b	0.50	0.89	0.020	0.035
b3	4.95	5.46	0.195	0.215
c	0.46	0.61	0.018	0.024
c2	0.46	0.89	0.018	0.035
D	5.33	6.22	0.210	0.245
D1	4.57	6.00	0.180	0.236
E	6.35	6.73	0.250	0.265
E1	3.81	6.00	0.150	0.236
e	2.29 BSC		0.090 BSC	
H	9.40	10.41	0.370	0.410
L	0.90	1.78	0.035	0.070
L3	0.89	2.03	0.035	0.080
L4		1.02		0.040
θ	0°	8°	0°	8°

RECOMMENDED LAND PATTERN

