SOP-8 Plastic-Encapsulate MOSFETS

SI4430

N-Channel Enhancement Mode Power MOSFET

Description

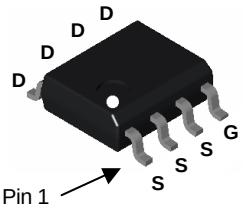
The SI4430 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge . The complementary MOSFETs may be used to form a level shifted high side switch, and for a host of other applications.

General Features

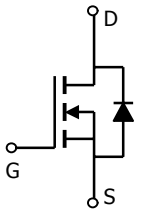
PRODUCT SUMMARY		
V_{DSS}	I_D	$R_{DS(on)}$ (mΩ) Max
30V	15 A	8.0 @ V_{GS} = 10V
	12 A	11.0 @ V_{GS} = 4.5V

- High power and current handing capability
- Lead free product is acquired
- Surface mount package

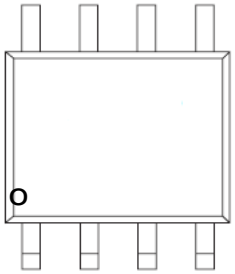
SO-8L



Equivalent Circuit



MARKING



Y :year code W :week code

Absolute Maximum Ratings T_A=25°C unless otherwise noted				
Parameter		**Symbol**	**Maximum**	**Units**
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current [A]	T_A=25°C	I_D	15	A
Pulsed Drain Current [B]		I_{DM}	75	
Power Dissipation [A]	T_A=25°C	P_D	3.0	W
	T_A=70°C		1.8	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics					
Parameter		**Symbol**	**Typ**	**Max**	**Units**
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	31	40	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		59	75	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	16	24	°C/W

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Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D= 250μA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}= 24V, V_{GS}=0V			500	nA
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±20V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D= 250μA	1.0	1.8	2.5	V
$I_{D(ON)}$	On state drain current	V_{GS}= 10V , V_{DS}= 5V			75	A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}= 10V, I_D= 15A		6.5	8.0	mΩ
		V_{GS}= 4.5V, I_D= 12A		9.0	11.0	mΩ
g_{FS}	Forward Transconductance	V_{DS}= 5V, I_D= 15A		29		S
V_{SD}	Diode Forward Voltage	I_S= 3A , V_{GS}=0V		0.76	1.0	V
I_S	Maximum Body-Diode Continuous Current				5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=25V, f=1MHz		6060		pF
C_{oss}	Output Capacitance			638		pF
C_{rss}	Reverse Transfer Capacitance			355		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz			0.9	Ω
SWITCHING PARAMETERS						
Q_g (10V)	Total Gate Charge (10V)	V_{DD}= 15V, V_{GEN} = 10V, I_D= 15A		103		nC
Q_g (4.5V)	Total Gate Charge (4.5V)			48		nC
Q_{gs}	Gate Source Charge			18		nC
Q_{gd}	Gate Drain Charge			15		nC
$t_{D(on)}$	Turn-On DelayTime	V_{DD}= 15V, V_{GEN}= 10V,R_L= 0.8Ω R_{GEN}=3Ω I_D= 15A		12		ns
t_r	Turn-On Rise Time			8		ns
$t_{D(off)}$	Turn-Off DelayTime			51		ns
t_f	Turn-Off Fall Time			8.8		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F= 18A, dI/dt=100A/μs		33		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F= 18A, dI/dt=100A/μs		22		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

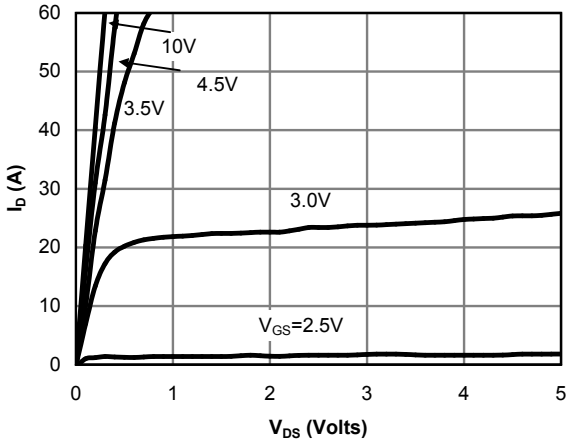

Fig 1: On-Region Characteristics

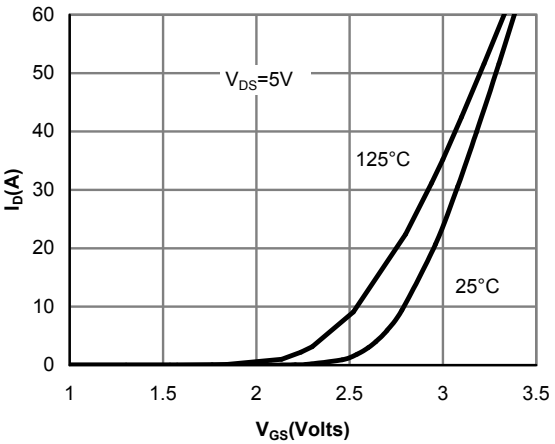

Figure 2: Transfer Characteristics

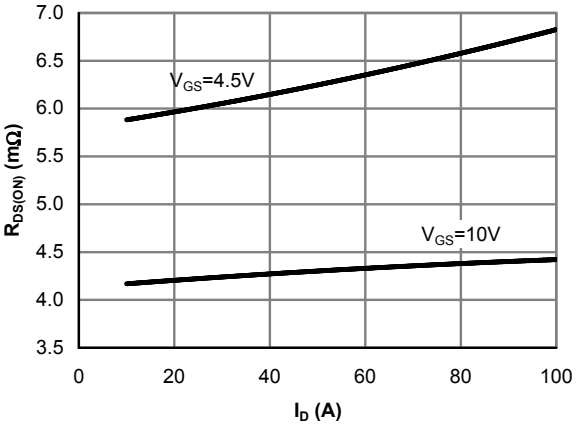

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

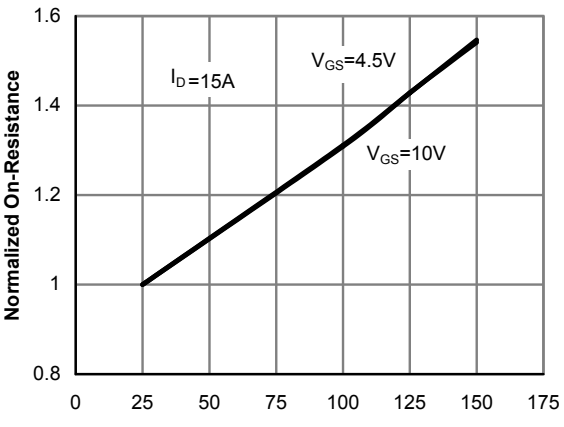

Figure 4: On-Resistance vs. Junction Temperature

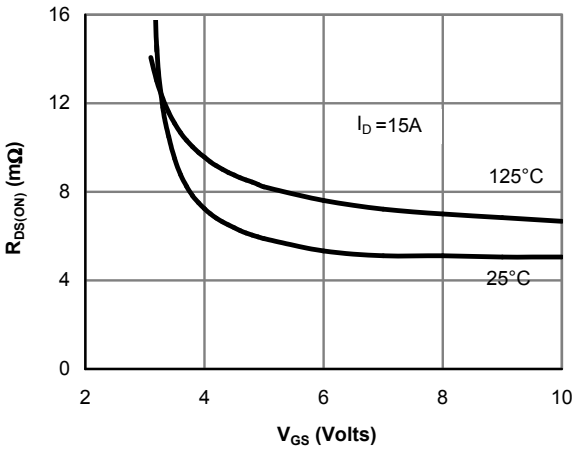

Figure 5: On-Resistance vs. Gate-Source Voltage

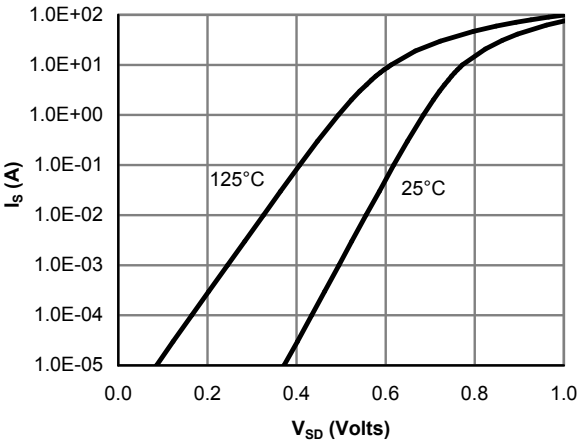

Figure 6: Body-Diode Characteristics

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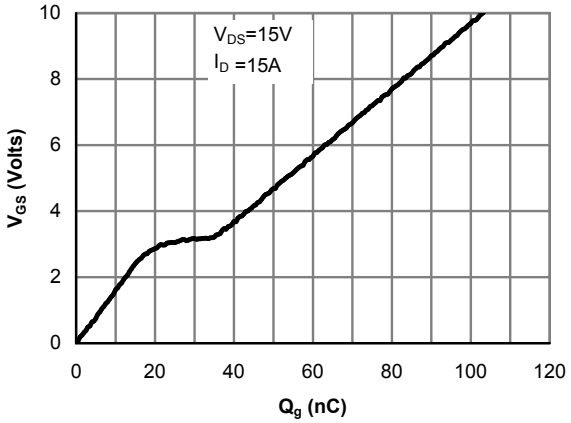

Figure 7: Gate-Charge Characteristics

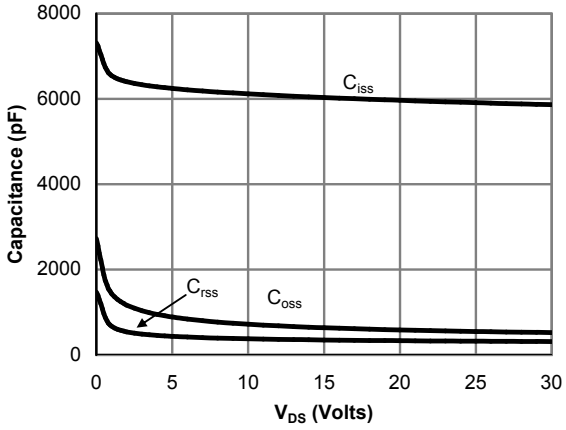

Figure 8: Capacitance Characteristics

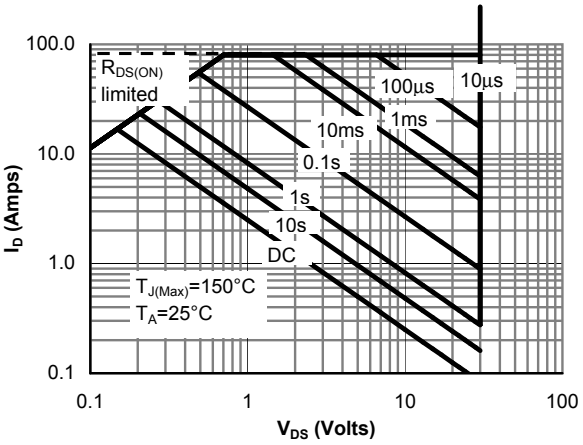

Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

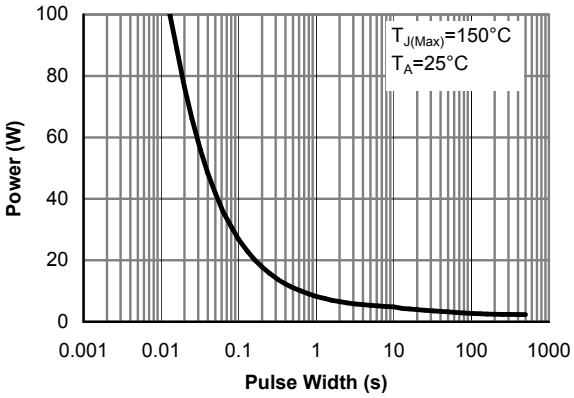

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

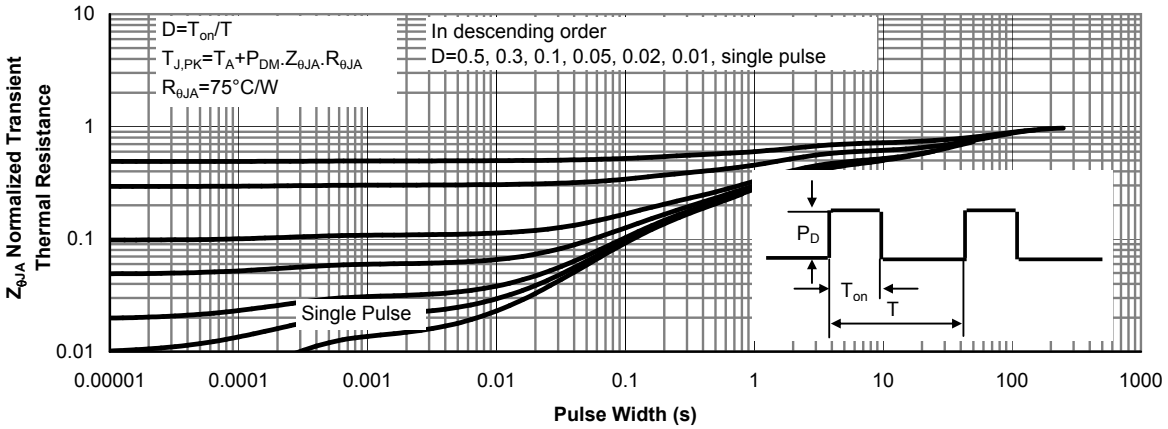

Figure 11: Normalized Maximum Transient Thermal Impedance

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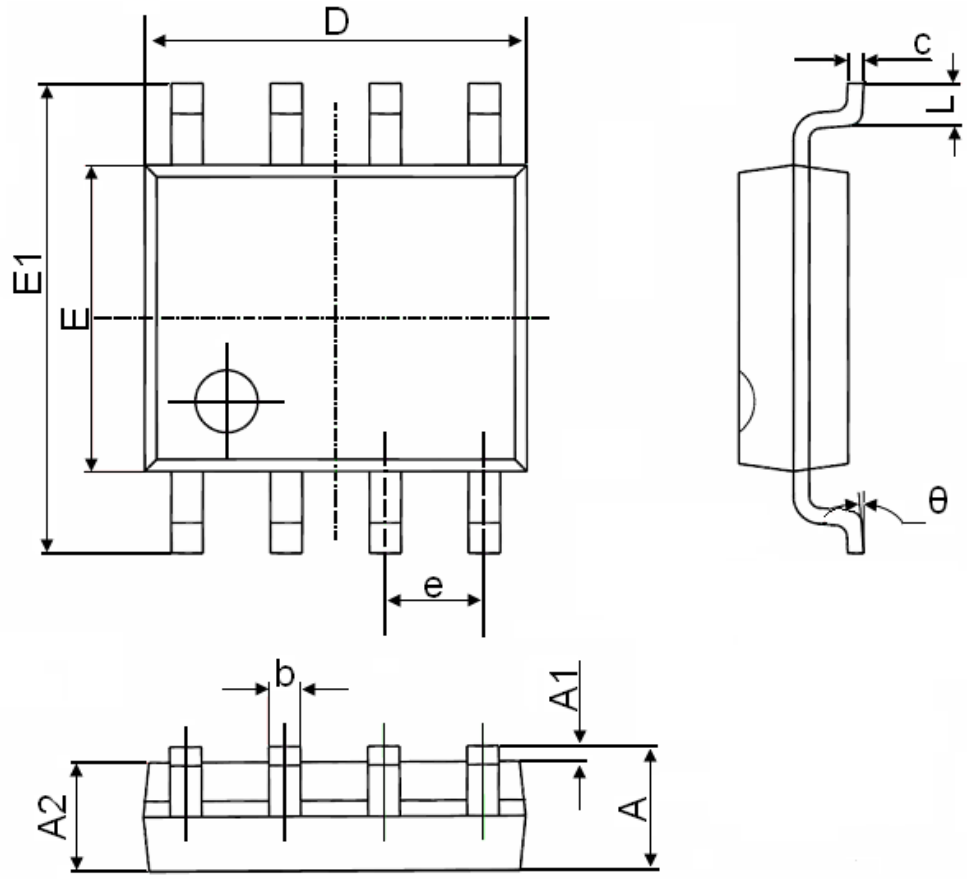
SOP-8 Package Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°